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AI-04-11: Report on acquisition test results on BepiColombo breadboard from 10 dBHz (TBC) to 27 dBHz for the 3 Titsworth schemes identified

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1. Introduction

This paper provides some trade-offs analysis and the preliminary breadboard results obtained in the frame of the ESA contract for the predevelopment of BepiColombo transponder.

2. The Titsworth Codes and JPL Approach (JPL 1999)

The Titsworth's approach has been selected by NASA's Jet Propulsion Laboratory (JPL) as baseline for regenerative ranging scheme (see DSMS Telecommunication Link Design Handbook 810-005 @ http://deepspace.jpl.nasa.gov/dsndocs/810-005/station/station_data.html).

The Titsworth's scheme is summarized hereafter in Figure 2-1.

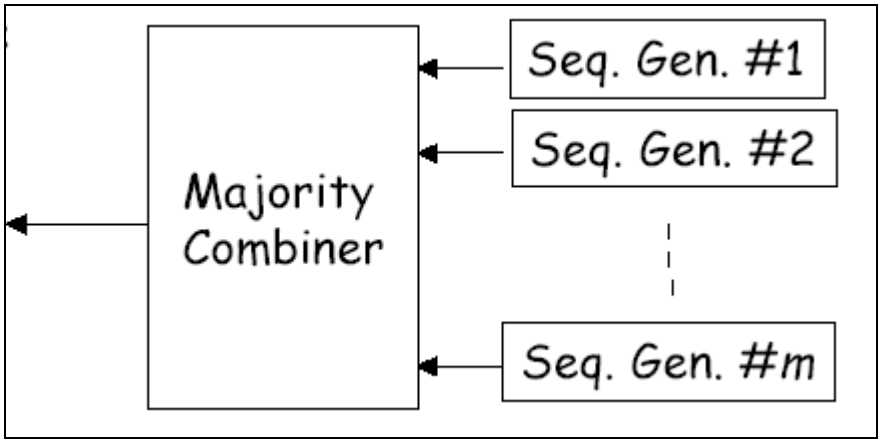


Figure 2-1 *Titsworth's scheme*

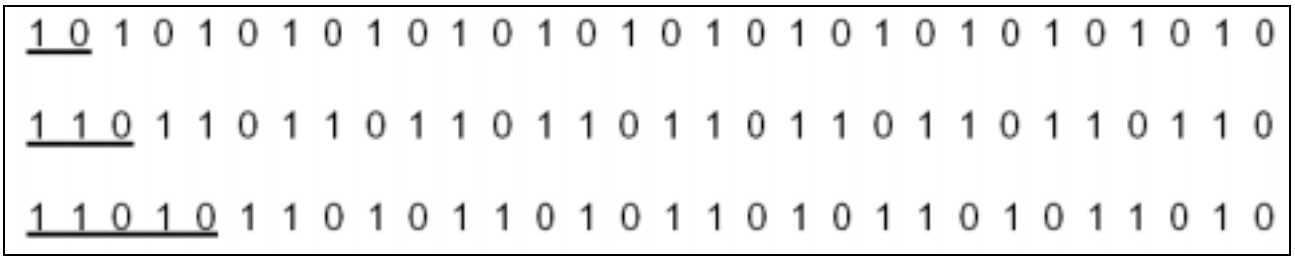
Note that the period T of the PN sequence obtained with the Titsworth's scheme is given by:

$$T = LCM(T_1, T_2, ..., T_m) \tag{2-1}$$

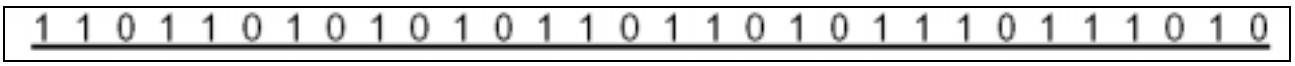
being LCM (T_1, T_2, …, T_m) the *least common multiple* of the component sequences periods T_1, T_2, …, T_m.

[1] The contribution of Alenia Spazio to this paper is based on the analysis and breadboard activity performed in the frame of the ESA contract for BepiColombo transponder predevelopment.

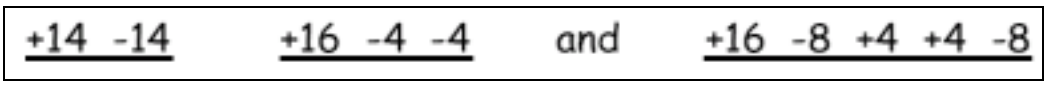
As an example, the following sequences of period 2, 3 and 5, respectively (the first period of each sequence is underlined):



combined by majority logic give the following period-30 sequence:



The correlation of this sequence (considered as +/-1 sequence) with the component sequences gives the periodic sequences reported hereafter:



Note that only **2 + 3 + 5 = 10 correlations** are required instead of the **30 correlations** needed in the "classical" approach. In fact, only 9 decisions are required because of a very useful property of the sequence of period-2. The two values of the correlation of this sequence with any periodic sequence are negatives of one another. Hence only one of the two correlations must be performed because the other correlation will be the negative of the one first performed.

The Titsworth's PN sequence proposed by JPL for regenerative ranging applications (indicated as JPL 1999 for short) is made up of six component of lengths 2, 7, 11, 15, 19, 23. The component sequences are as follows:

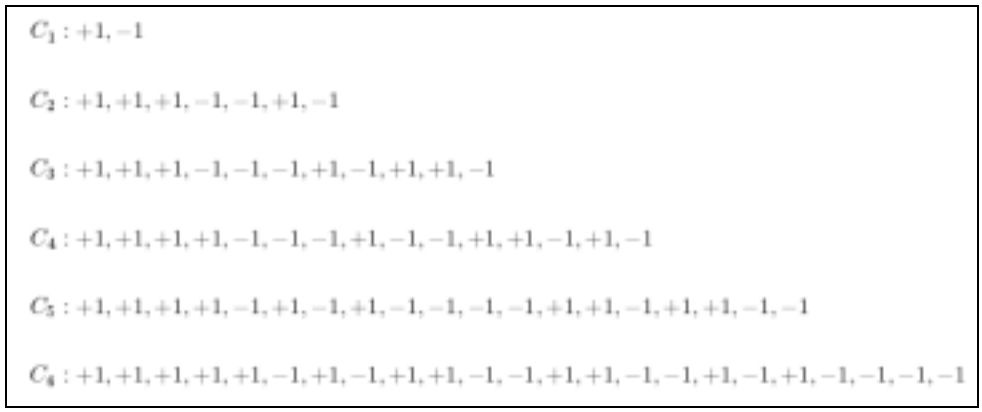


Table 2-1 *JPL 1999: code components*

The first component C_1 is identified as clock component.

The JPL 1999 ranging sequence is built by AND'ing components C_2 through C_6 and OR'ing the result with the clock component C_1 (assuming that –1 maps to logical '0' and +1 maps to logical '1'). The resulting sequence length is the product of the six sequence lengths, i.e. 1,009,470 chips.

The JPL 1999 is a particular Titsworth scheme, using the same components C1…C6 (in the following sometimes indicated also as sub-sequences) but applying different voting rule for the clock we can build different Titsworth codes (see para.3 in the following).

The statistical properties of the JPL 1999 code have been investigated with the help of a dedicated MATLAB program.

Distribution of '+1' and '-1

It results:

$$\sum_{i\ \text{even}} Seq(i) = 504{,}375$$
$$\sum_{i\ \text{odd}} Seq(i) = -458{,}655$$

Since half the sequence length is 504,735, this means that, for *i* even, the sequence is always +1, and, for *i* odd, there are 481,695 –1's and 23,040 +1's. Therefore, the sequence is very similar to an alternating +/1 pattern.

Correlation of the sequence with the components

Let define Cor (*n*,*m*) the correlation of the n^{th} component with the entire sequence offset by *m* chips, i.e.:

$$\text{Cor}(n,m) = \sum_{i=0}^{1{,}009{,}469} Seq(i+m)C_n(i) \qquad (2\text{-}2)$$

The above relationship gives the following results:

- Cor(1,0) = 963,390
- Cor(1,1) = -963,390
- Cor(*n*,0) = 46,080 for *n*=2,..,6
- Cor(*n*,*j*)=0 for *n*=2,..,6 and $j \neq 0$

Therefore, for components C_2 to C_6, only one offset value has a non-zero correlation. In addition, the majority of the energy is in the clock component, which will aid in acquisition of the sequence during the regeneration process.

3. Modified JPL's PN Ranging Codes

The PN regenerative ranging scheme outlined in the previous section can be modified by changing the rule for forming the ranging sequence from the six component sequences C_1, C_2, C_3, C_4, C_5 and C_6 to the following:

Combine the chips of the six periodic component sequences at the same position by weighted voting with C1 given 4 votes (V=4) and the other sequences 1 vote each. It is indicated in the following as Titsworth V4 for short

Table 3-1 – *Titsworth V4*

The correlations of C_1, C_2, C_3, C_4, C_5 and C_6 with one period (1,009,470 chips) of this +1/-1 ranging sequence are as follows:

C_1:	942600	-942600
C_2:	66870	-6930 -6930 -6930 -6930 -6930 -6930
C_3:	66870	-4158 -4158 -4158 -4158 -4158 -4158 -4158 -4158 -4158 -4158
C_4:	66870	-2970 -2970 -2970 -2970 -2970 -2970 -2970
		-2970 -2970 -2970 -2970 -2970 -2970 -2970
C_5:	66870	-2310 -2310 -2310 -2310 -2310 -2310 -2310 -2310 -2310 -2310
		-2310 -2310 -2310 -2310 -2310 -2310 -2310 -2310
C_6:	66870	-1890 -1890 -1890 -1890 -1890 -1890 -1890 -1890 -1890 -1890
		-1890 -1890 -1890 -1890 -1890 -1890 -1890 -1890 -1890 -1890
		-1890 -1890

Table 3-2 *Titsworth V4**:** Correlations of the component sequences with one-period code for the combining rule in Table 3-1*

On the basis of the correlations reported in the table above, it results that with this approach the clock component is virtually as strong as it is in the ranging scheme JPL 1999. On the other hand, the peaks relevant to the correlation of the component from C_2 to C_6 with one period sequence are well above those obtained with the original scheme (JPL 1999).

Another promising alternative to JPL1999 is the following:

Combine the chips of the six periodic component sequences at the same position by weighted voting with C1 given 2 votes and the other five sequences 1 vote each. It is indicated in the following as Titsworth V2 for short

Table 3-3 – *Titsworth V2*

In this case, the correlations of the component sequences with the +1/-1 ranging sequence are as follows:

C_1:	623400 -623400
C_2:	261510 -26906 -26906 -26906 -26906 -26906 -26906
C_3:	259374 -15930 -15930 -15930 -15930 -15930 -15930 -15930 -15930 -15930 -15930
C_4:	257910 -11274 -11274 -11274 -11274 -11274 -11274 -11274 -11274 -11274 -11274 -11274 -11274 -11274
C_5:	256926 -8714 -8714 -8714 -8714 -8714 -8714 -8714 -8714 -8714 -8714 -8714 -8714 -8714 -8714 -8714
C_6:	256230 -7098 -7098 -7098 -7098 -7098 -7098 -7098 -7098 -7098 -7098 -7098 -7098 -7098 -7098 -7098 -7098

Table 3-4 *Titsworth V2: Correlations of the component sequences with one-period code for the combining rule in Table 3-3*

According to the results presented in Table 3-4, the C_1 power reduces by 3.8 dB with respect to the JPL 1999. However, the power of the component from C_2 to C_6 increases by 15.2 dB, approximately.

4. Breadboard Description

The three different Titsworth schemes, above introduced (JPL 1999, Titsworth V4 and Titsworth V2), have bee implemented in the BepiColombo breadboard and they are under testing in Alenia Spazio laboratory.

The regenerative ranging channel operations are accomplished in two stages: the received ranging signal is first acquired in phase and once this has taken place, the ranging code is tracked.
There are primarily two philosophies with regard the tracking of digital ranging signal. The so-called *direct* tracking approach makes direct use of the correlation properties of the code itself to provide an error signal when the received code tends to drift from the delayed locally generated replica of the code. The second method includes in the ranging signal format a clock component that the ranging receiver locks onto by means a dedicated phase-locked loop (the chip tracking loop). The clock estimate formed in the chip-tracking loop drives a code generator, which produces a local replica of the code.

The regenerative ranging channel designed for the BepiColombo breadboard is designed using this second approach due to the fact that the selected PN ranging code contains a strong clock component (i.e. the period-2 component sequence)[2]. According to the block diagram showed in Figure 4-1 the regenerative ranging channel includes the following signal processing functions:

1. Chip Tracking Loop for ranging code clock component (i.e. the code chip) phase and frequency recovery;
2. Six Correlators running in parallel for ranging code sequences position recovery;
3. Code Generator;
4. Control Logic for correlators and code generator management;

[2] The level of the clock component is different for the three different Titsworth schemes.

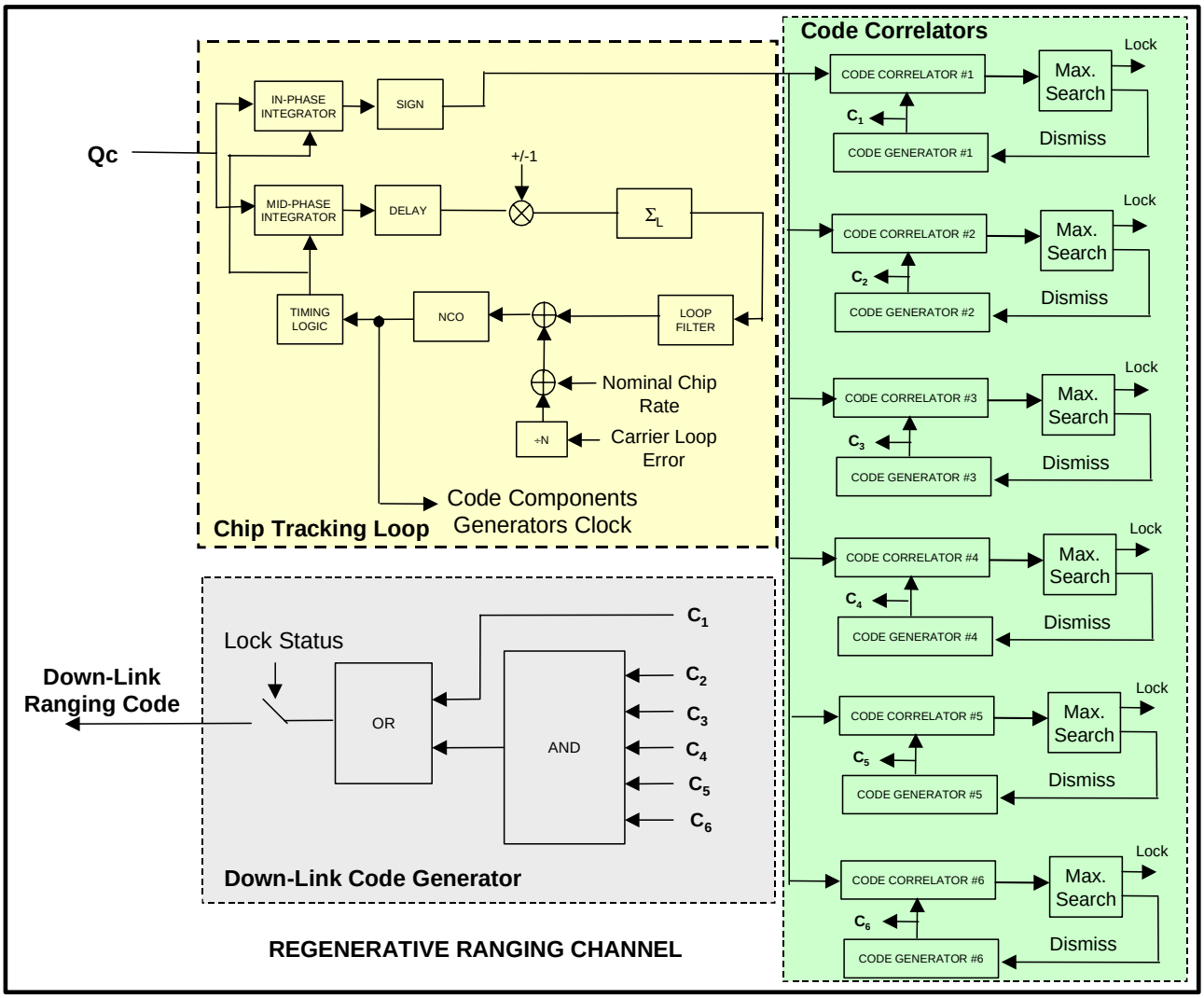


Figure 4-1 Regenerative ranging based on PN sequence: JPL1999 block diagram

The PN ranging code resembles a square-wave with a few "errors". Therefore the Chip Tracking Loop (CTL) is designed modifying a Data Transition Tracking Loop (DTTL). The in-phase integrator is controlled by the CTL NCO and it delivers to the Code Component Correlators the hard-quantized chip. The filtered loop error is summed to the Base Frequency term (corresponding to the nominal chip rate) and the result is used to control the NCO frequency.

It is good to have the ranging signal clock component coherently related to the transmitted carrier frequency; in this case it is possible to apply an *aided acquisition* scheme for proper CTL synchronization. With this approach, the CTL NCO Base Frequency is obtained summing the nominal chip rate with the carrier loop error scaled by the ratio of the ranging chip rate by the up-link carrier frequency. This second term offers an estimation of the Doppler on the ranging signal and allows improving the CTL acquisition performance due to the fact that only the chip phase (not the frequency) must be recovered. The CTL NCO output frequency is used to drive the shift registers, which generate the six code components in the Code Generator blocks.

The Chip Tracking Loop (CTL) is based on the block diagram showed in Figure 4.2.

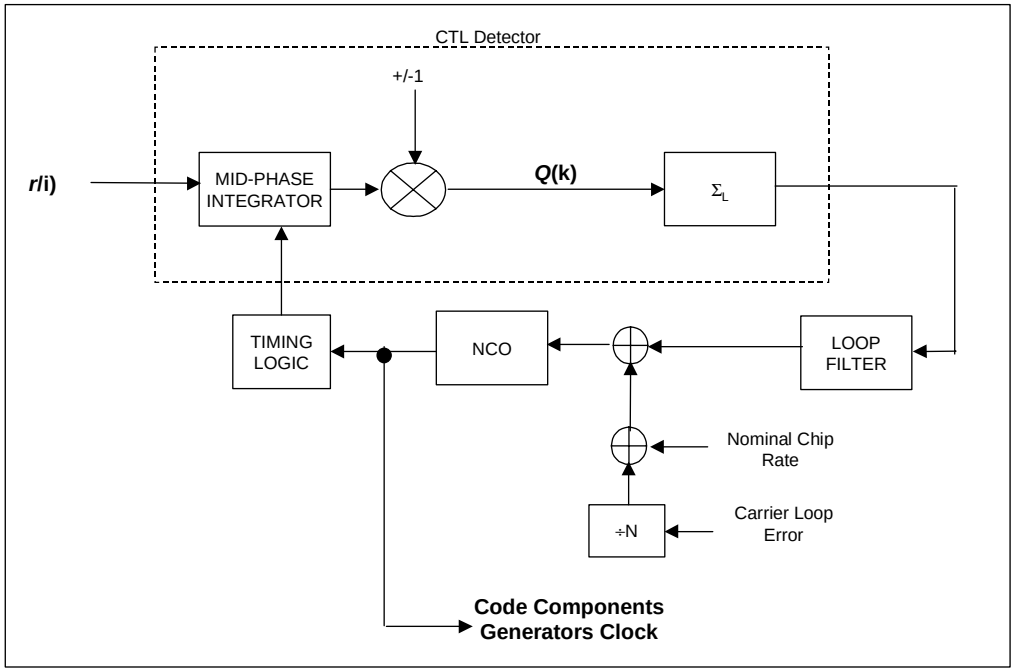


Figure 4.2 CTL block diagram

The acquisition of each *Ci* components is performed in parallel (6 correlators). The strategy is based on the "Maximum Search" or selection of the largest correlation value. It means that for each component the algorithm will evaluate the correlation output for the different possible phases (23 possible phases for C6, 19 for C5, etc). The selected phase for each component will corresponds to the largest value.

5. Trade-off Analysis

Based on the above (Alenia breadboard) block diagram and for the different Titsworth codes above defined, we have performed the following analyses for the evaluation of

- the code acquisition time
- tracking jitter performances.

5.1 Acquisition Time

In the following we apply the same analysis introduced by JPL in the two papers:

- TMO Progress Report 42-137 Regenerative Pseudo-Noise Ranging for Deep Space applications (May15, 1999)
- Operations Comparison of Deep Space Ranging Types: Sequential Tone vs Pseudo-Noise.

This analysis is based on the search of the maximum at the output of the correlator for each sub-sequence. The same approach above described and applied by Alenia in BepiColombo breadboard.

JPL calculates the integration time for JPL1999 only for Pr/No=27 dBHz. We have found a small discrepancy with respect to the value *T(1)....(*T6) reported in page 9 of the TMO paper. For instance *T(6)* is 17.46 sec at 27 dBHz instead of 17.19 sec.

It is understood that, the integration time *T(i)* corresponds to the acquisition time of the sub-sequence *Ci* only in case of parallel processing for each sub-sequence; it means 23 correlators for *C6*, 19 for *C5*, etc. This is not clearly indicated in the TMO paper.

In a more realistic approach for on-board application[3], we have to consider just one correlator for each sub-sequence (see block diagram of Alenia breadboard above reported). Of course this is not the optimum choice in terms of acquisition time, which is related to the longest component (C6).

Note that the acquisition time for each sub-sequence *Tacq(Ci)* has been defined as:

- *Tacq(Ci) = Length(Ci)*T(i)*
- *Length(Ci)* = sub-sequence length or number of different chip/phase to be tested (for instance 23 for C6, 19 for C5, etc)
- *T(i) = integration time for each* chip/phase to be tested

So increasing the energy of the longest component (C6) with proper voting (see the case with majority voting 2 for *C1*) we expect a drastically reduction of the overall acquisition time. This is good for the acquisition of the phase, but of course this must be paid in terms of clock synchronization (less energy on the clock component).

This behaviour is confirmed in the figure 5-1, where Pacq=0.999 is related to the probability of acquisition for the overall code.

[3] Of course for G/S application we can propose and implement solutions based on a higher level of parallelized processing.

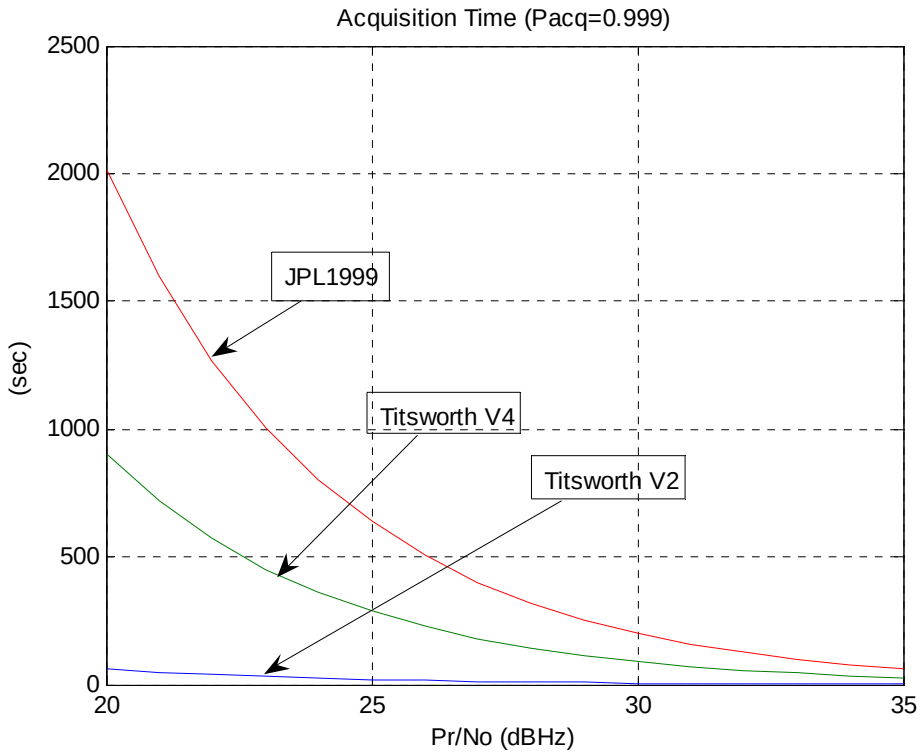


Figure 5-1. *Acquisition time performances for the different Titsworth schemes.*

Note that this analysis is based on the Alenia breadboard architecture and takes into account only the acquisition of the phase of the code assuming a perfect synchronism in the acquisition tracking of the chip rate. As result we can see that:

- The Titsworth V4 scheme shows an acquisition time shorter (about ½) than the JPL1999 still keeping almost the same power level for the clock component.
- For low Pr/No only the Titsworth V2 scheme gives acceptable performances (note that 1000÷2000 sec might have a non negligible impact in terms of S/C operations), but in this case the clock component is much smaller and this will reduce the chip loop tracking performances.

Applying the same terminology used in the TMO progress report and assuming that the code acquisition time is basically the time needed to acquire the longest component[4] (C6) we have:

- **Tc/Ta**=((Cmax_a - Cmin_a)/(Cmax_c - Cmin_c))^2= ((46080-0)/(256230+7098))^2= **0.0306**
- **Tb/Ta**=((Cmax_a - Cmin_a)/(Cmax_b - Cmin_b))^2= ((46080-0)/(66870+1890))^2=**0.449**

Where:

– **a** is related to JPL1999, **b** to Titsworth V4 and **c** to Titsworth V2
– Cmax is the maximum normalised correlation value
– Cmin is the minimum normalised correlation value

At the reference value[5] of 27 dBHz (Ec/No = - 33 dB for a chip rate of 1 Mcps) we have: Ta (JPL 1999) ≈ 400 sec, Tb (Titsworth V4) ≈ 180 sec, Tc (Titsworth V2) ≈ 13 sec.

[4] This is valid for the acquisition scheme implemented by Alenia for BepiColombo breadboard.
[5] The same reference value used in the TMO Progress Report.

5.2 Tracking Jitter Analysis

As reference to the Chip Tracking Loop (CTL) above described we have performed the following analysis. The signal at the CTL input is derived form the carrier quadrature channel (inside the digital demodulator section) and it can be expressed as:

$$r(i) = r(it_s) = A\sum_k a_k \cdot p(it_s - kT - \tau) + N_i \tag{5.2-1}$$

Where:

- t_s is the sampling interval;
- A is the amplitude of the chip;
- T is the chip time;
- N_i is zero mean white Gaussian noise sample with variance:

$$\sigma_i^2 = \frac{N_0}{2t_s} \tag{5.2-2}$$

- τ is the random epoch to be estimated;
- $p(t_i)$ is the square-wave function having a value of 1 for $0 \le t_i \le T$ and having value 0 elsewhere, i.e.:

$$p(it_s) = \text{rect}\left(\frac{it_s}{T}\right)$$

- a_k represents the kth chip polarity.

We assume that the input symbols have their leading edge at $\ldots kT + \tau, (k+1)T + \tau, \ldots$, and that the loop generates its leading edges at $\ldots kT + \hat{\tau}, (k+1)T + \hat{\tau}, \ldots$so the timing error ε is:

$$\varepsilon = \tau - \hat{\tau} \tag{5.2-3}$$

Now we determine the tracking performance of the CTL in terms of timing jitter, namely σ_ε^2.

Using linear theory, σ_ε^2 can be derived once the following two quantities are determined:

1. the loop *S*-curve;
2. the two-sided spectral density of the equivalent additive noise.

The *S*-curve is defined as the mean value of the error control signal conditioned on the timing error. Mathematically, we have:

$$S(\varepsilon) = L \cdot E(Q_k | \varepsilon) \tag{5.2-4}$$

Where $E(\bullet)$ denotes the statistical expectation, ε is expressed by the (5.2-3), Q_k is the quadrature channel output (see Figure 4.2 above) and L represents the accumulation length of the integrate-&-

dump following the quadrature branch of the CTL. The mid-phase integrator output is given by (see Figure 4-2):

$$Q_k = \sum_{i \in C_k} r(i) = \sum_{i \in C_k} \{A[a_k \cdot p(it_s - kT - \tau)] + N_i\} \tag{5.2-5}$$

Where:

$$C_k = \left\{ i : \left(k - \frac{1}{2}\right)T + \hat{\tau} \le it_s < \left(k + \frac{1}{2}\right)T + \hat{\tau} \right\} \tag{5.2-6}$$

The mid-phase integrator output is multiplied by +/-1 in order to provide the right correction to the loop. In a certain way the multiplication by +/-1 replaces the transition detector considering that the PN sequence resembles a square-wave. The mean value of the mid-phase integrator output after multiplication by +1/-1 is easily found (see also Figure 5.2):

$$E(Q_k) = 2A \cdot \left(\frac{\varepsilon}{t_s}\right) \tag{5.2-7}$$

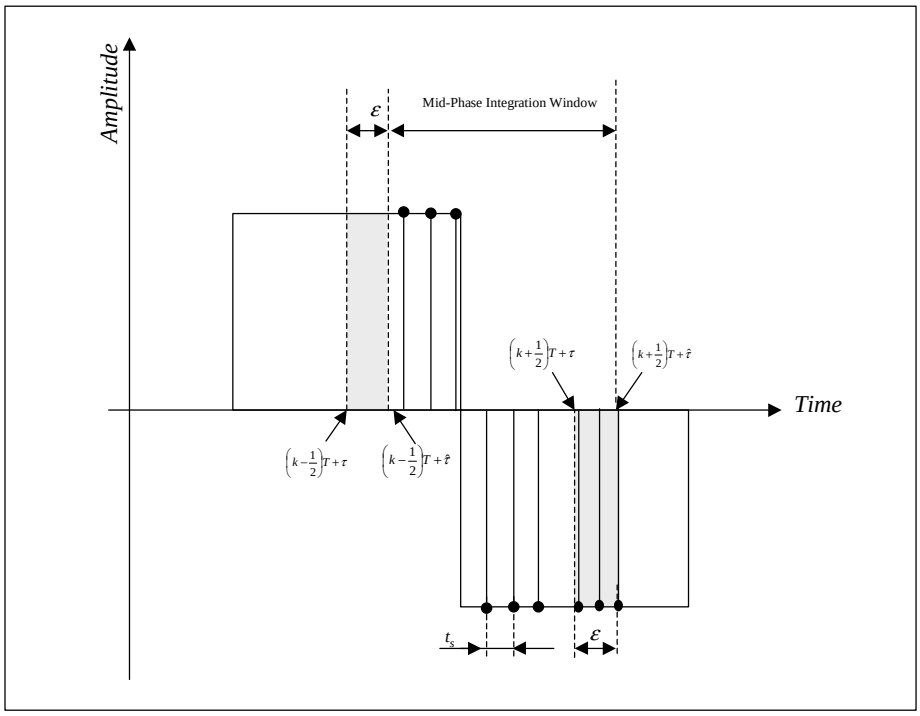


Figure 5.2 *Depiction of the mid-phase integration*

Substituting the above relationship into equation (5.2-4) offers:

$$S(\varepsilon) = 2AL\left(\frac{\varepsilon}{t_s}\right) \tag{5.2-8}$$

We point out that the obtained relationship for the *S*-curve is meaningful when the loop is in tracking. Besides, due to discrete nature of the accumulation, ε is always quantized to an integer multiple of the

sampling period t_s; however, the presence of noise makes the quantization effect negligible, if the number of samples per chip is high enough. The slope of the *S*-curve at the origin represents the loop detector gain K_ε:

$$K_\varepsilon = \left.\frac{\partial S(\varepsilon)}{\partial \varepsilon}\right|_{\varepsilon=0} = \frac{2AL}{t_s} \tag{5.2-9}$$

To evaluate the loop equivalent additive noise, we assume the CTL in tracking ($\varepsilon \to 0$). Under this assumption the variance at the phase detector output is:

$$\sigma_N^2 = L \cdot \mathrm{Var}(Q_k) = L \frac{N_0}{2t_s}\left(\frac{T}{t_s}\right) = L \cdot \frac{N_0 T}{2t_s^2} \tag{5.2-10}$$

The loop timing jitter σ_ε^2 can be estimated using a linearized model of the CTL. With this approach, the loop error η at the phase detector output can be written as:

$$\eta = K_\varepsilon \cdot \varepsilon + N \tag{5.2-11}$$

being *N* the additive Gaussian noise with variance expressed by the equation (5.2-1). The above relationship leads to the equivalent linearized loop reported in Figure 5.3.

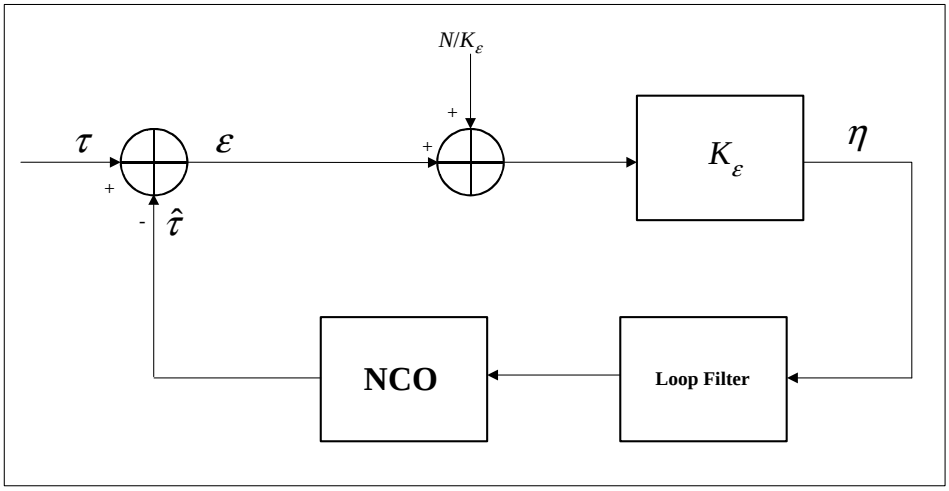


Figure 5.3 Linearized loop model (synchronization error expressed as *timing* error)

From the general theory of PLL we have:

$$\sigma_\varepsilon^2 = \frac{\left(\frac{S_N}{2}\right) \cdot 2B_L}{K_\varepsilon^2} \tag{5.2-12}$$

Where B_L is the loop bandwidth and S_N is the spectral density of the additive noise in the loop, that is:

$$\frac{S_N}{2} = \sigma_N^2 \cdot (L \cdot T) = L^2 \cdot \frac{N_0 T^2}{2t_s^2} \tag{5.2-13}$$

Substituting the (5.2-10) and the (5.2-13) into (5.2-12), we find:

$$\sigma_\varepsilon^2 = \frac{\left(L^2 \cdot \frac{N_0 T^2}{2t_s^2} \right) \cdot (2B_L)}{\left(\frac{2AL}{t_s} \right)^2}$$

From which:

$$\sigma_\varepsilon^2 = \frac{1}{4} \cdot \frac{B_L \cdot T^2}{(P_r / N_0)} \tag{5.2.14-a}$$

Where $\frac{P_C}{N_0} = \frac{1}{T} \cdot \frac{E_c}{N_0}$ is the ranging clock component power-over-noise spectral density ratio, being E_c/N_0 the energy chip-over-noise spectral density ratio equal to A^2T (i.e. $P_c=A^2$). In practice, it is convenient to express the loop jitter normalizing with respect to the chip phase error ϕ by letting:

$$\phi = 2\pi \frac{\tau - \hat{\tau}}{T} = 2\pi \frac{\varepsilon}{T}$$

Thus:

$$\sigma_\phi^2 = 4\pi^2 \frac{\sigma_\varepsilon^2}{T^2}$$

From which we find the CTL signal-to-noise ratio ρ as:

$$\rho = \frac{1}{\sigma_\phi^2} = \frac{1}{\pi^2} \cdot \left(\frac{P_c}{N_0} \right) \cdot \left(\frac{1}{B_L} \right) \tag{5.2-14-b}$$

As an example, for $P_r / N_0 = 30$ dBHz and considering a CTL loop bandwidth of 2 Hz the relationship (5.2-14) gives 17 dB as signal-to-noise ratio inside the CTL.

As already mentioned, in the above relationship, P_c/N_0 shall be intended as the C_1 clock component power over noise spectral density ratio. In section 6.2, the theoretical expectations are compared with the test results.

6. Test Results

6.1 Spectral characteristics

The RF spectrum of the PN Regenerative Ranging has been measured using an all-digital modulator. The modulated carrier frequency is equal to 10 MHz (a 40 MHz clock is used to synchronize the FPGA-device) and the chip rate was chosen equal to 2.5 Mchip/s.

The un-filtered spectra for the three different Titsworth schemes (JPL1999, Titsworth V4 and Titsworth V2) are presented in the following pages for various frequency spans. Note that for all of them, we have applied the same modulation index of 1 radiant peak.

As general comment we can underline the following:

- strong clock component at 1.25 MHz;
- sin*x*/*x* shape due to effect of the longer repetition components that determine the pseudo-randomness of the code;
- discrete component at integer multiple of the clock rate
- different power distribution for the PN code components for the different codes (due to different majority voting weight).

In the following table (Table 6.1) we summarise, for each Titsworth scheme, the main spectral characteristics referred to the level of the residual carrier:

- the level of the code-clock component
- and the level of the worst code component in the band of the TC signal (around 16 KHz in this case) .

Note that all the plots and the summary results reported in the next table are related to a carrier modulation index of 0.82 rad-pk.

	Clock component referred to the residual carrier (dBc)	**Worst case spectral component in the TC bandwidth referred to the residual carrier (dBc)**	**Noise floor in the TC bandwidth referred to the residual carrier (dBc/Hz)**
JPL 1999	-4.1	-47	-78
Titsworth V4	-4.3	-42	-76
Titsworth V2	-7.8	-36	-72

Table 6.1- *Summary of the spectral characteristics for the three Titsworth schemes.*

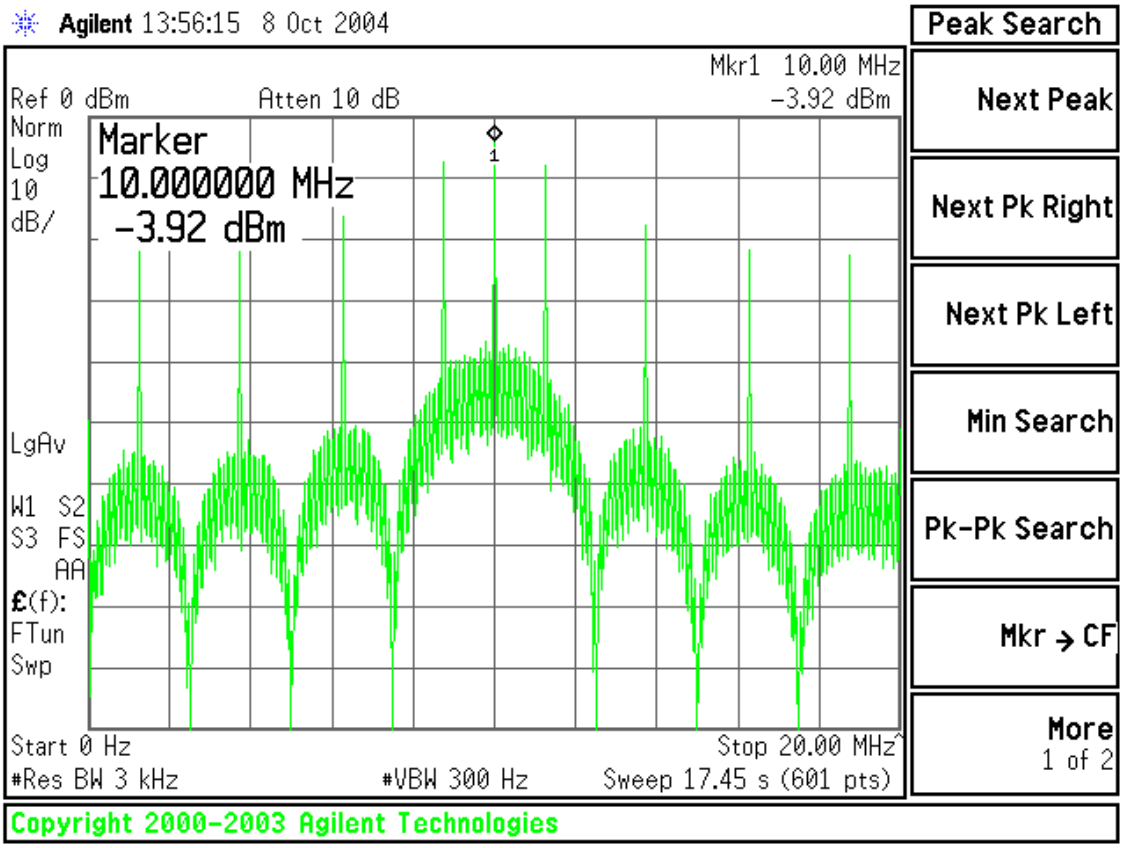


Figure 1 – JPL 1999 ranging spectrum (1/5)

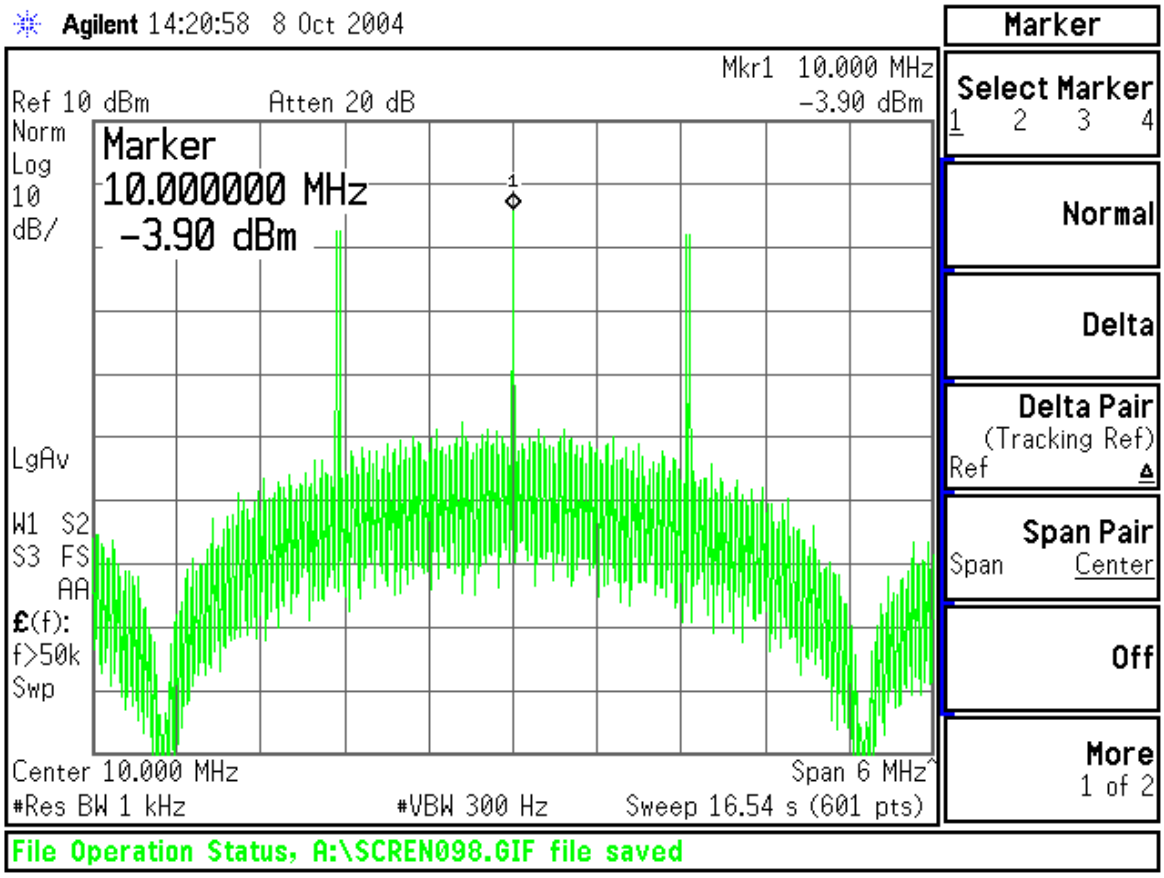


Figure 2– JPL 1999 PN ranging spectrum (2/5)

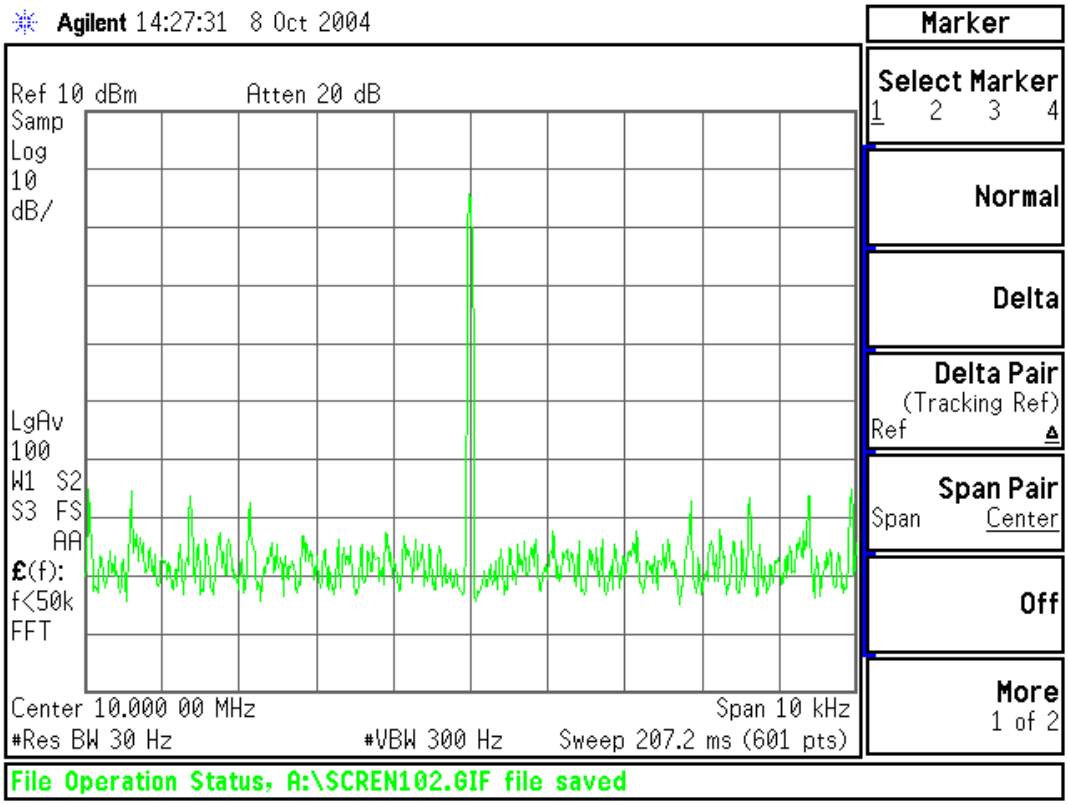


Figure 3 – JPL 1999 PN ranging spectrum (3/5)

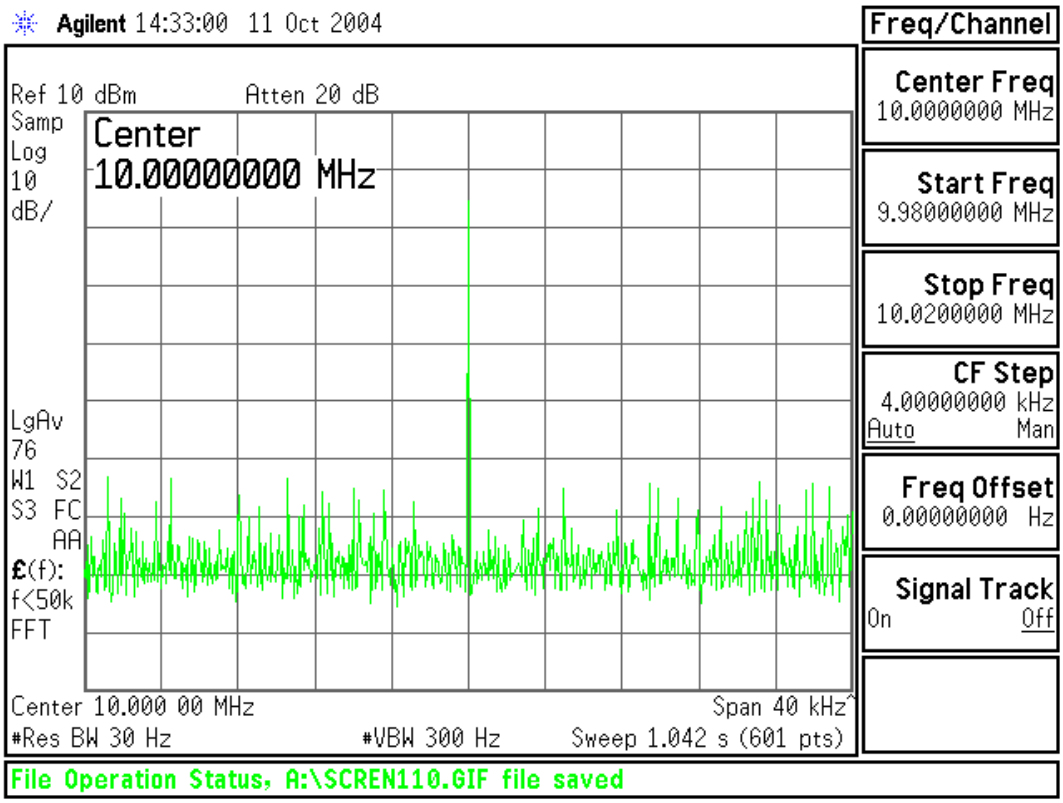


Figure 4 – JPL 1999 PN ranging spectrum (4/5)

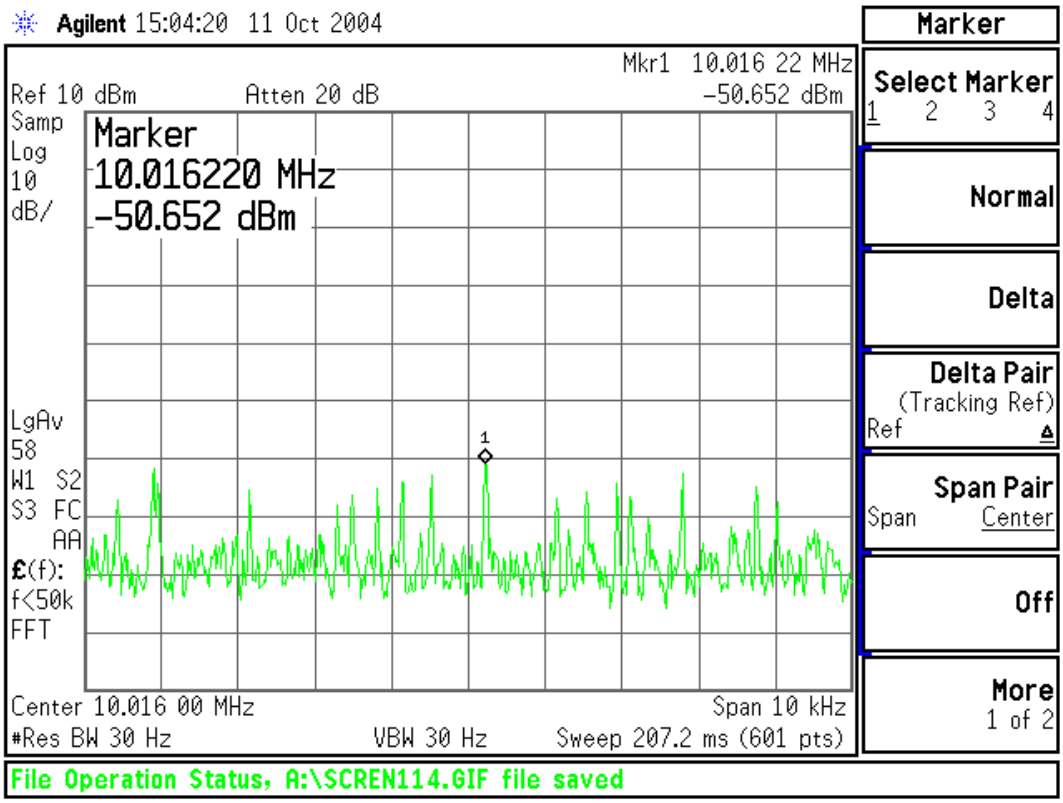


Figure 5 – JPL 1999 PN ranging spectrum (5/5)

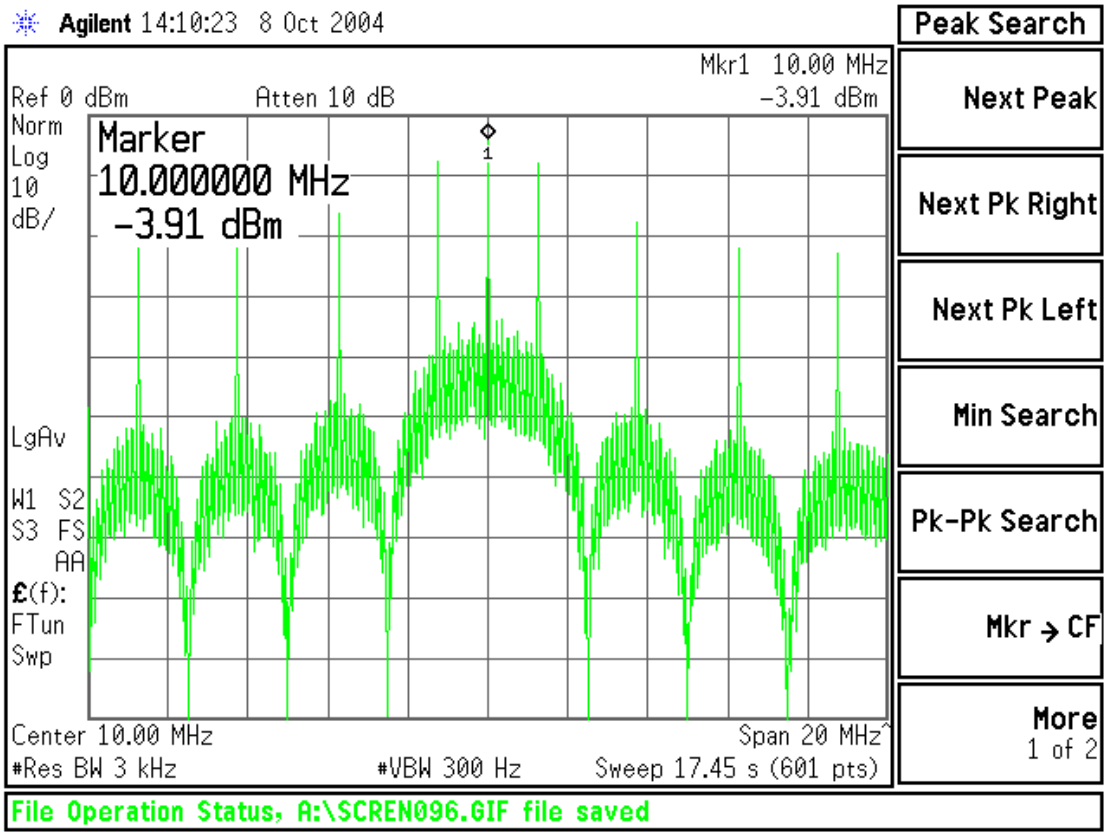


Figure 6 – Titsworth V4 PN ranging spectrum (1/5)

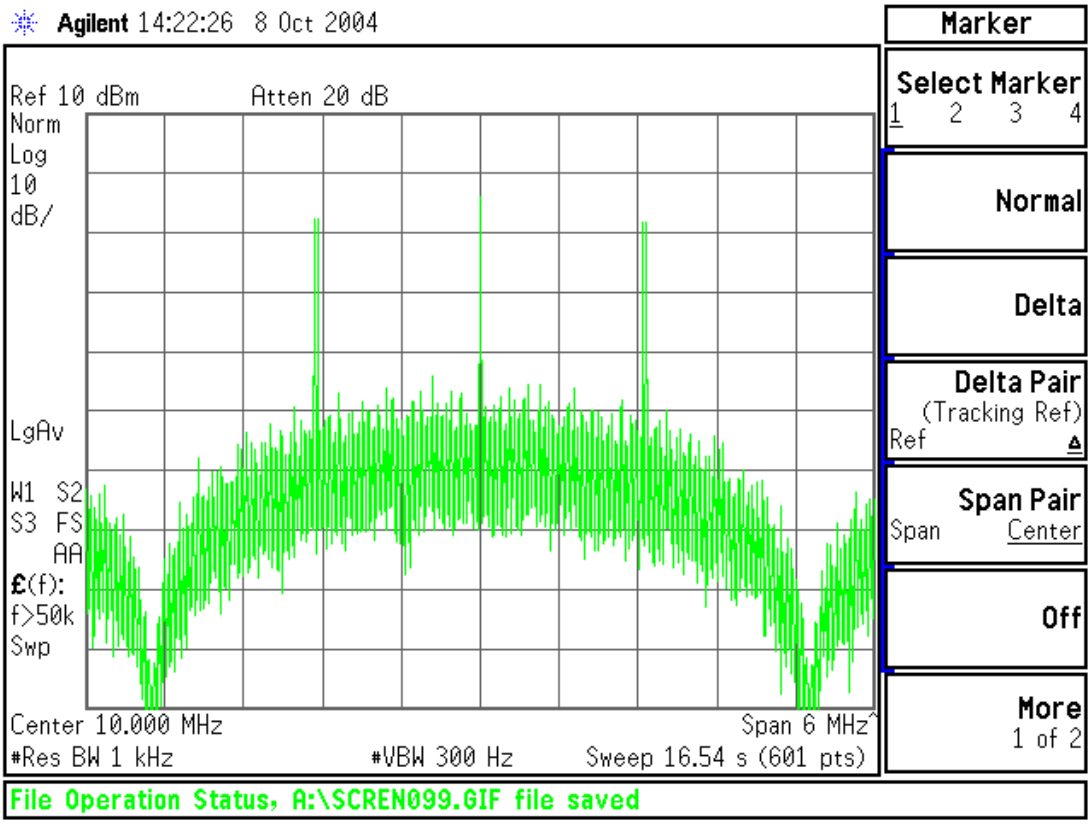


Figure 7 - Titsworth V4 PN ranging spectrum (2/5)

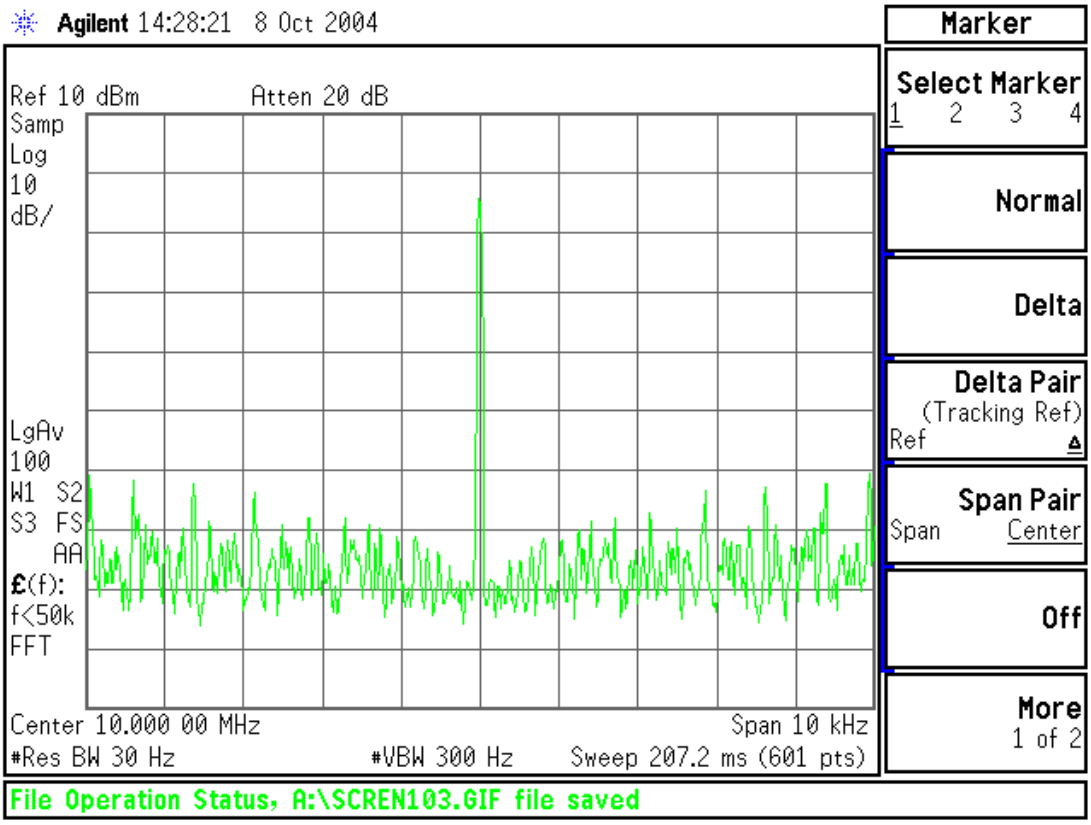


Figure 8 - Titsworth V4 PN ranging spectrum (3/5)

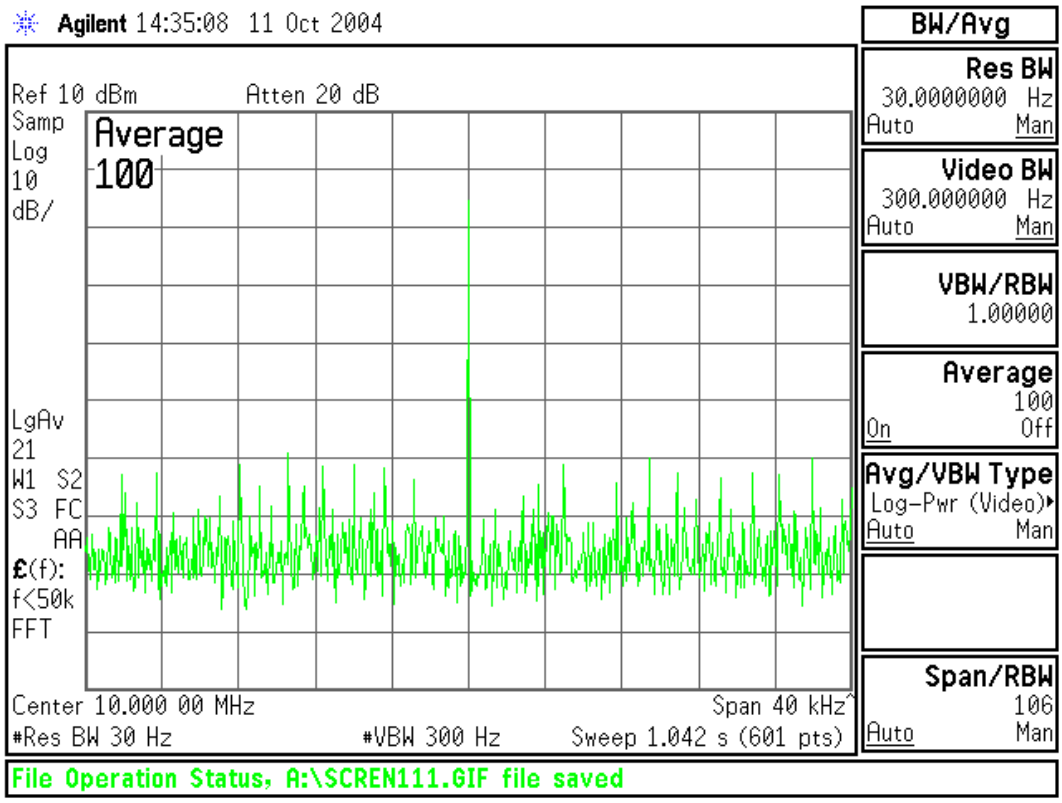


Figure 9 – Titsworth V4 PN ranging spectrum (4/5)

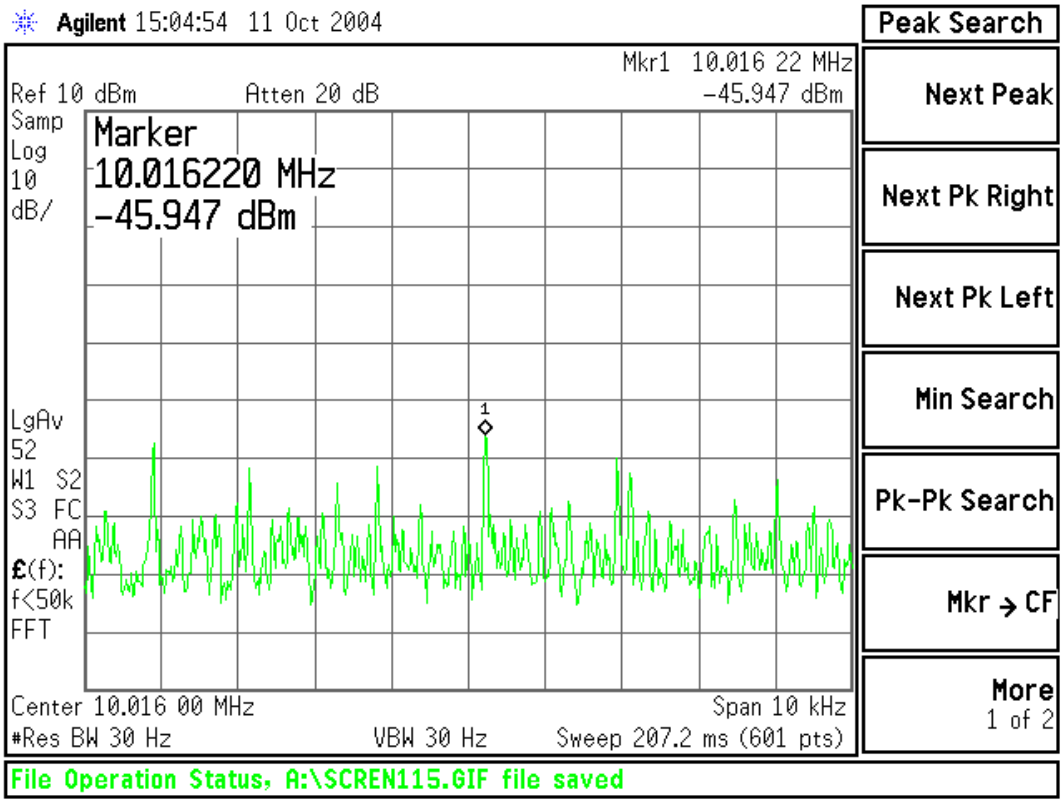


Figure 10 – Titsworth V4 PN ranging spectrum (5/5)

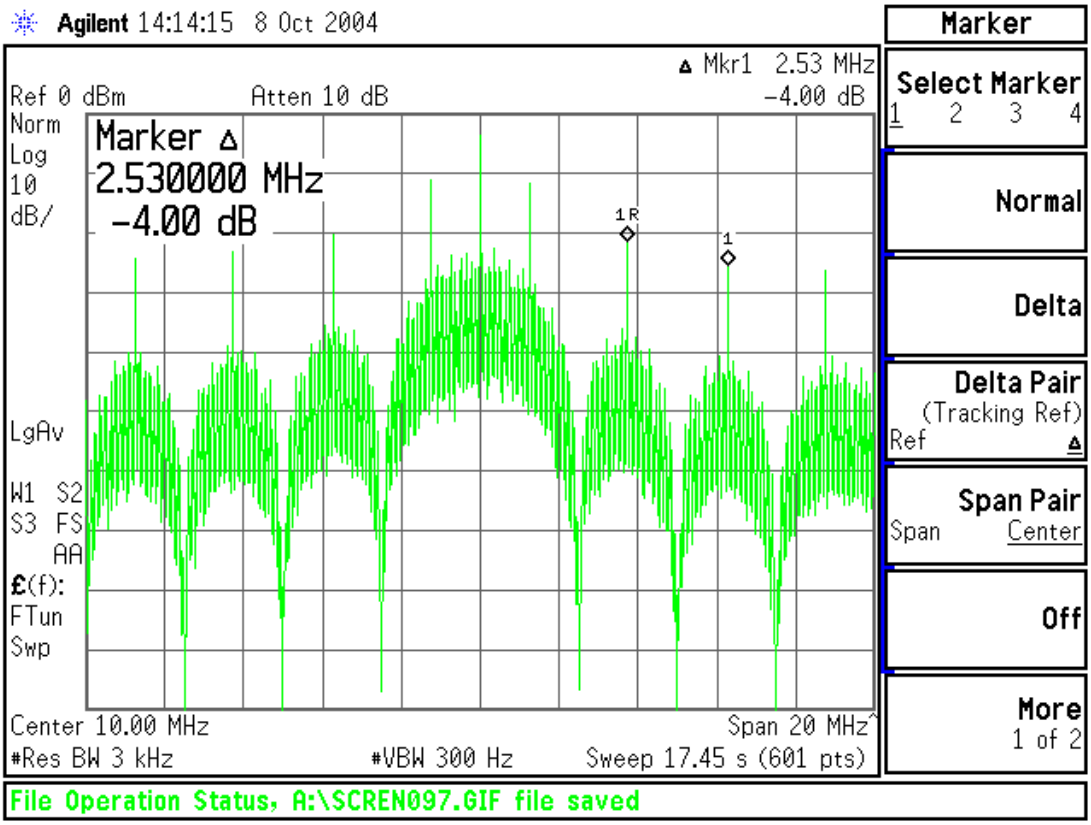


Figure 11 - Titsworth V2 PN ranging spectrum (1/5)

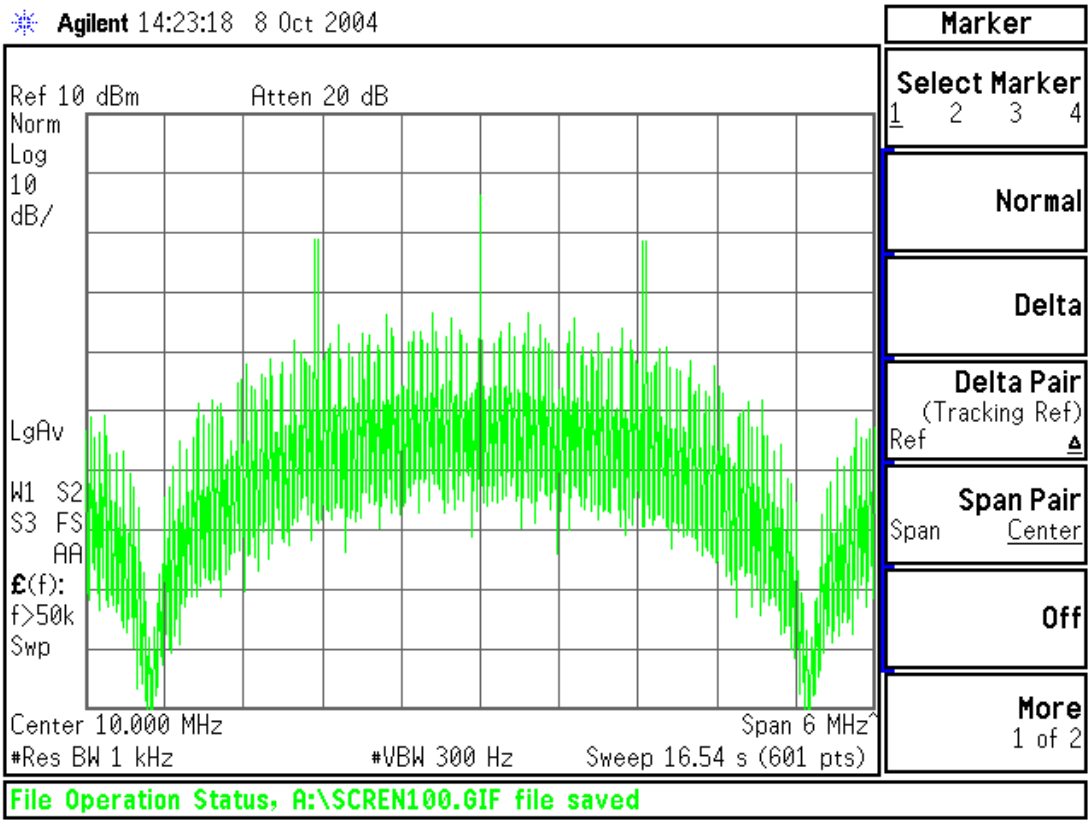


Figure 12 - Titsworth V2 PN ranging spectrum (2/5)

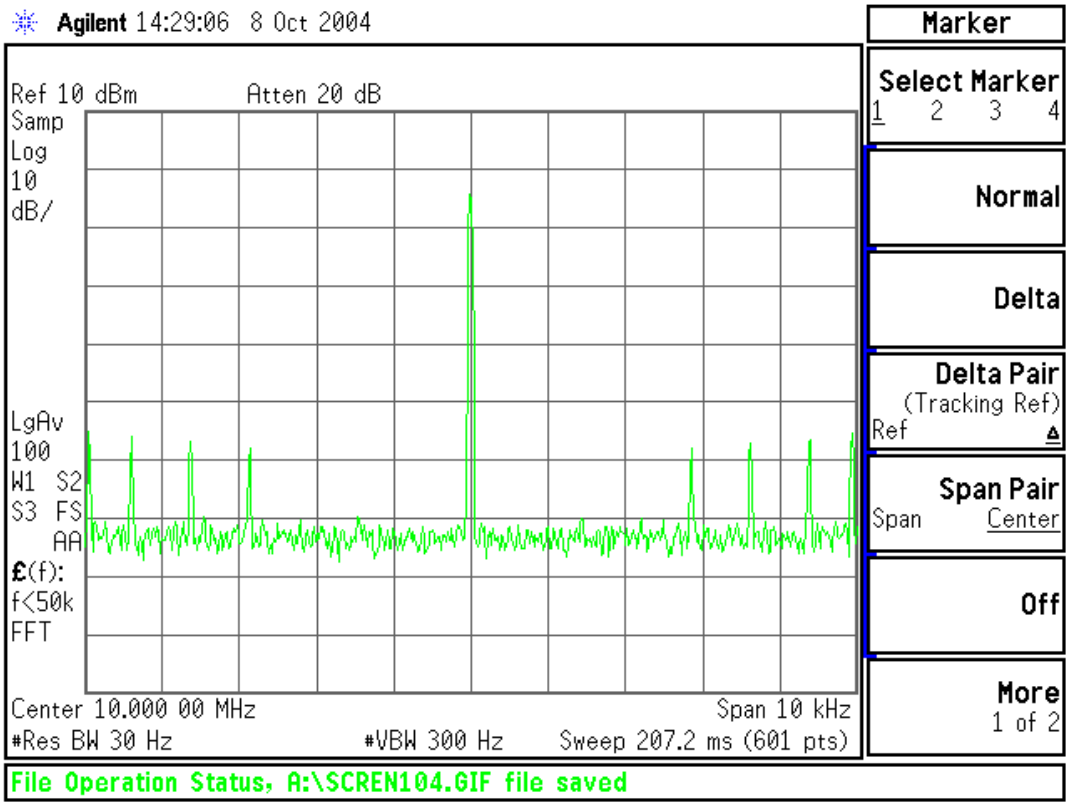


Figure 13 - Titsworth V2 PN ranging spectrum (3/5)

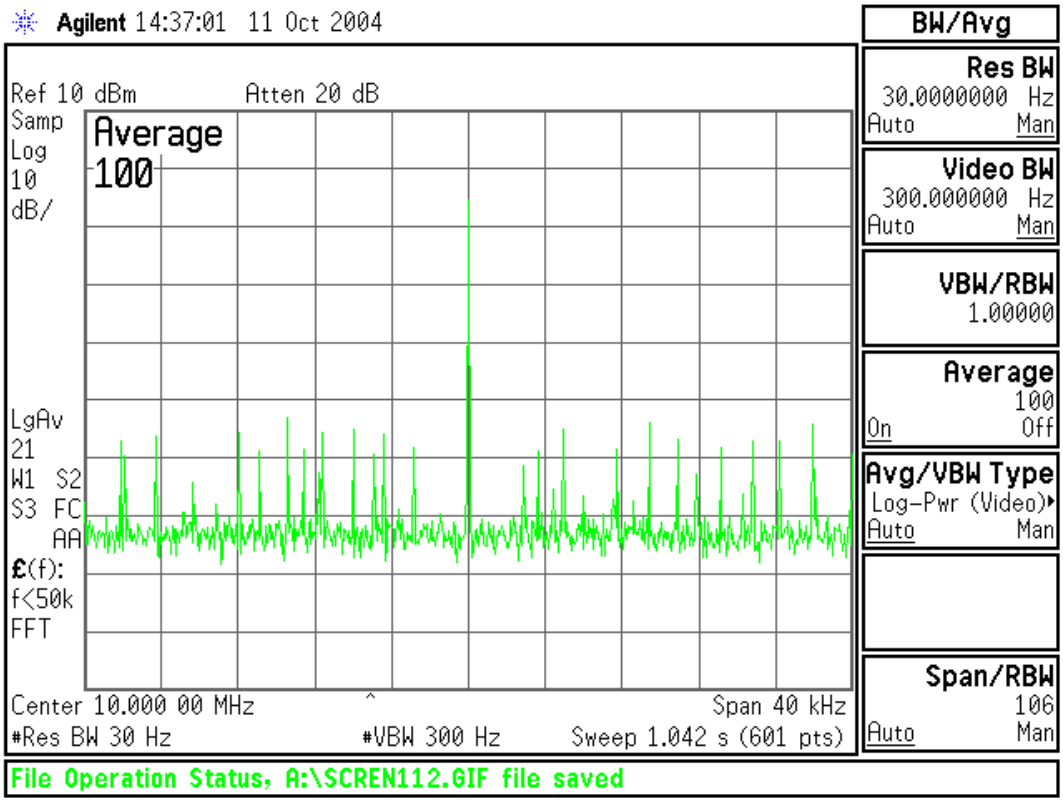


Figure 14 – Titsworth V2 PN ranging spectrum (4/5)

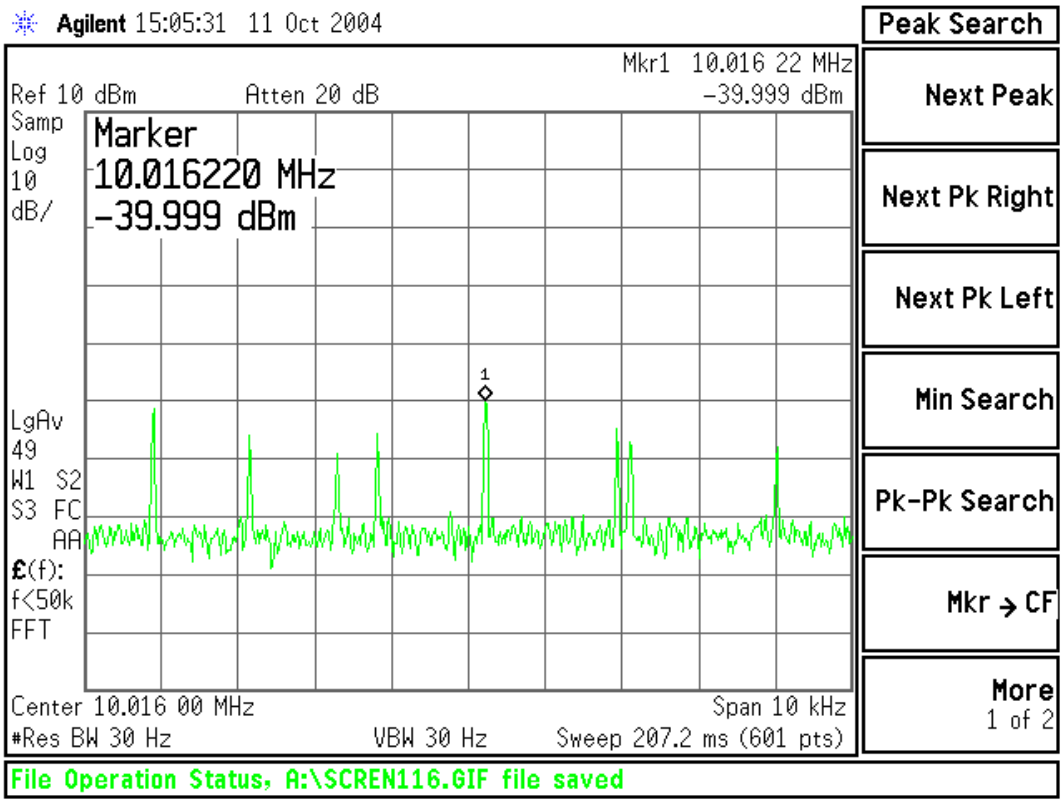


Figure 15 – Titsworth V2 PN ranging spectrum (5/5)

6.2 Statistics and Tracking performances

A test campaign has been performed in order to investigate the correlation properties of the Titsworth codes above defined. The PN ranging receiver correlators output have been measured as function of the ranging power-over-noise spectral density ratio (i.e. Pr/No). The correlation window has been programmed equal to 5 periods of the overall sequence corresponding to 5 sec at the selected chip rate of 1 Mchip/s. Clearly, it is possible to extend the integration process in order to improve the acquisition of the code component from C_2 to C_6.
The test results are summarised hereafter (see Table 2.1-1) for JPL 1999 code and for the modified JPL codes using a majority-voting equal to 4 and 2 respectively. The test results are provided as C_i (i=1,2,…6) correlator output versus Pr/No.

JPLL 1999

Pr/No (dBHz)	C_1	C_i (i=2,3,4,5,6)	Jitter (ns pk-pk)
39	400000	30000	85
33	200000	not meas.	125
27	65000	not meas.	200

Titsworth V4

Pr/No (dBHz)	C_1	C_i (i=2,3,4,5,6)	Jitter (ns pk-pk)
39	400000	37000	85
33	190000	12000	125
27	60000	not meas.	200

Titsworth V2

Pr/No (dBHz)	C_1	C_i (i=2,3,4,5,6)	Jitter (ns pk-pk)
39	260000	160000	130
33	112000	70000	160
27	tracking loss		

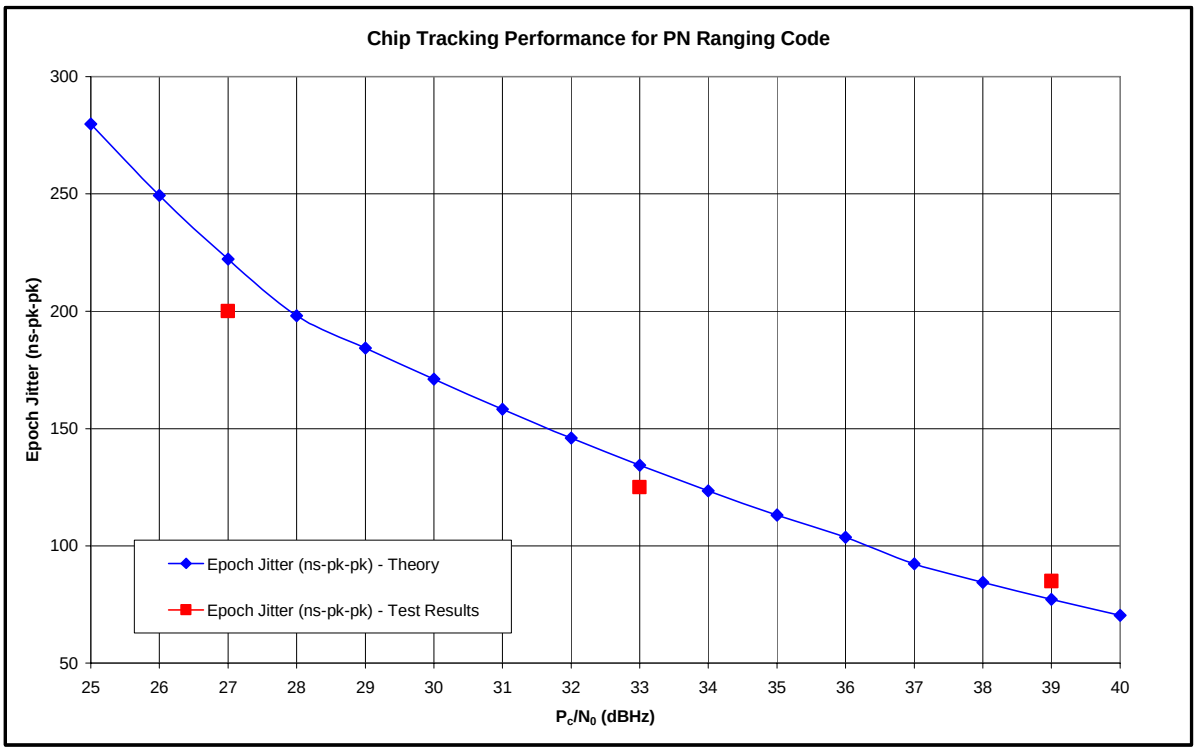
Table 6-1 *Test results (chip rate = 1 Mchip/s)*[6]

The test results are in line with the theoretical expectation as reported in the previous section. It is worthwhile to mention that at Pr/No=27 dBHz the code synchronisation performance when using a majority voting equal to 2 (Titsworth V2) could be enhanced by improving the relevant tracking loop design (see the note on the chip tracking steady state error in the following).

The loop tracking jitter measured during the breadboarding activity has been compared with the theoretical figure expressed by (5.2-14). As it is shown in the following plot, a good matching between experimental results and theoretical expectation has been found. Note that:

- Pc/No is practically equal to Pr/No for the case of JPL 1999 and Titsworth V4. In case of Titsworth V2, Pc/No reduces by 3.8 dB with respect to JPL 1999, keeping fixed the Pr/No.
- The CTL loop bandwidth is changing from about 11 Hz (at Pc/No=25 dBHz) up to 22 Hz (at Pc/No=40 dBHz)[7].

[6] "Not measurable" means that the correlator output variance is comparable with the correlator output peak.
[7] The CTL loop bandwidth must be optimized.



6.2.1 Note on Chip Tracking Loop Steady-State Error

The chip-tracking loop at present implemented in the BepiColombo breadboard is a first-order loop. In addition, the loop bandwidth is not controlled by a dedicated digital AGC and it varies according to the input signal strength. Any potential frequency error appears as a steady-state error in the tracking loop.

In particular, the chip-tracking loop NCO has a resolution of 9.5 Hz (frequency control word = 21 bit, clock frequency = 20 MHz); this digital round-off introduces a frequency error that leads to a steady-state error increasing as the input signal strength reduces. This effect has been clearly monitored during the test campaign on PN ranging.

In the next phase, this problem will be avoided applying the following approach based on:

- 28 bit NCO;
- Second-order loop for chip tracking

7. Conclusions

As above underlined, in the frame of the action item AI_04-11, there are several issues still open, in particular we have:

- Optimization of the chip tracking loop (CTL) performances and verification of the tracking threshold for the different Titsworth schemes,
- Code phase acquisition performances versus Pr/No for different Titsworth schemes with and without up-link Telecommand,
- Telecommand demodulation performances in presence of PN ranging for different Titsworth schemes.

The BepiColombo breadboarding activity will investigate also on these issues, which are considered crucial for the design and development of the new regenerative ranging system.