**SLS-RFM_23-05 CCSDS Action on Green Book Annex for GMSK/PN**

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## Introduction

This annex addresses concerns regarding the use of GMSK/PN in a high Doppler rate environment, i.e., when the signal experiences large frequency dynamics. Particularly, we look at the likelihood that the GMSK demodulator will lose carrier lock. To perform the analysis, we first need to define a carrier lock structure. We choose the maximum a-posteriori probability (MAP) carrier synchronizer which we describe now.

## Receiver Model

From [1], a receiver can be devised using an offset quadrature phase shift keying (OQPSK) architecture whose matched filters are designed using $C_0$ and $C_1$ Laurent pulse shapes. Since we are implementing $BT_S = 0.5$ and $BT_S = 0.25$ with a constrained complexity, our focus will be in developing carrier synchronization using only $C_0$. Our architecture is based on the low SNR implementation of the MAP carrier synchronizer [10]. Figure 1 shows a diagram of the carrier recovery loop. Complex envelope samples are passed through separate real and imaginary matched filters set to the $C_0$ pulse. There's an optional Wiener equalizer prior to the matched filters to mitigate intersymbol-interference produced when implementing only the $C_0$ pulse for $BT_S = 0.25$. The matched filter samples are then sent to a derotator whose function is to rotate the samples by a phase estimate, $\widetilde{\phi}$. Now there is some ambiguity with where the derotator should be placed either before or after the matched filters (and equalizer, if implemented). The placement of derotator affects the transfer function of the loop due to delay from the matched filters. When the derotator is before the matched filter as indicated in dashed lines, additional delays are incurred in the closed loop transfer function of the loop and thus the poles of the 2nd order loop are deviated from its design [3]. We refer to this as the optional architecture. To avoid this issue, the derotator can be placed after the matched filters as shown in solid lines. However, there is the issue of the additional delay incurred from the matched filter on the data samples. The loop will process this delayed data and possibly not correct signal dynamics properly. We call this the baseline architecture. We attempt to assess the impact to the system in either case, but we start with baseline first.

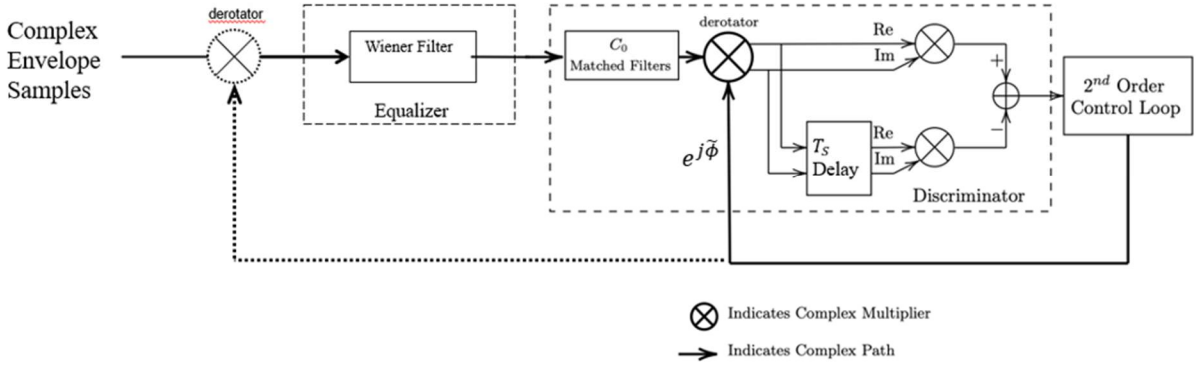


*Figure 1: Low SNR MAP Carrier Recovery Loop*

The derotation is accomplished by a complex multiplication of the samples with the exponential $e^{j\tilde{\Phi}}$. The complex result of the derotation is passed to a real multiplication of the real and imaginary components and a real multiplication of the real and imaginary components delayed by $T_S$. The multiplicative results are subtracted from each other according to the diagram. This creates a discrimination at only once per $2T_S$ time and the result are fed to a 2nd order control loop which is designed in the same manner as the phase locked loop found in [4], except that the input multiplier is replaced by the discriminator.

The discriminator gain, $K_d = 2S_d$, where $S_d$ is found in [5]:

$$S_d = (2E_S)^2 - \sum_{m=-\infty}^{\infty} h^2(m - 1/2),$$

$h(m)$ is the autocorrelation of the $C_0$ pulse, and $m$ is the index of the $m^{th}$ demodulated symbol.

The S-curve of the discriminator is defined as:

$$S(\theta) = S_d \sin 2\theta$$

which signifies a $180°$ phase ambiguity similar to a BPSK Costas loop or squaring loop. Figure 2 shows a simulation of the S-curve based on $C_0$ and the accuracy of the S-curve with $BT_S = 0.5$. As the plot shows, the prediction is exact. In this example, $S_d = 6.1162$.

Since the S-curve of the discriminator is a sine function, we can model the discriminator as a conventional phase detector used in phase-locked loops as shown in Figure 3.

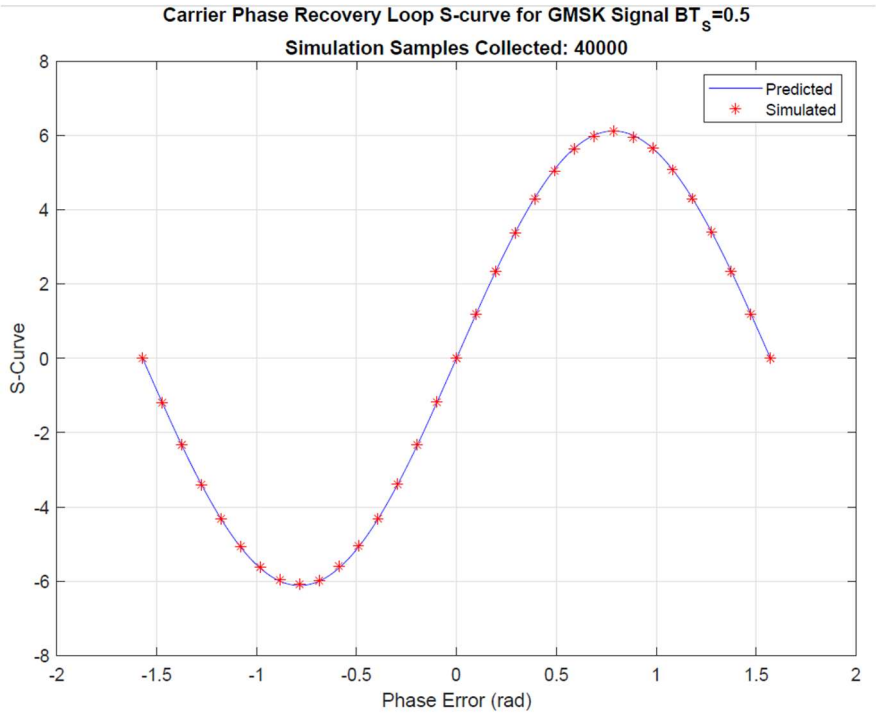


*Figure 2: S-curve based on $C_0$ pulse*

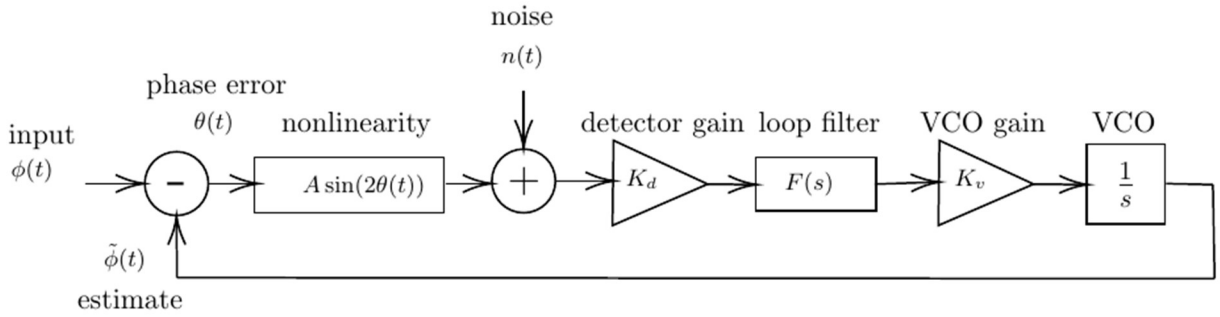


*Figure 3: Mathematical Model of Baseline Architecture*

Note that we have included details of the second order control loop such as the detector gain, loop filter, voltage control oscillator (VCO) gain and VCO. As mentioned before the control loop is designed in the conventional manner using an active proportional plus integrator. To model the behavior of this loop, we need to calculate the noise variance of the loop. We know that variance for $2\theta$ is [2]:

$$\sigma_{2\theta}^2 = \frac{4N_{B_L}}{\frac{E_S}{N_0}S_L} \tag{1}$$

where $E_S$ is the GMSK bit energy, $N_0$ is the noise density and $\frac{E_S}{N_0}$ is the GMSK bit signal-to-noise ratio (SNR). The ratio $N_{B_L} = \frac{B_L}{R_S}$ is called the normalized loop bandwidth where $B_L$ is the loop bandwidth and $R_S = 1/T_S$ is the GMSK bit rate. The $S_L$ term is called the squaring loss which is created by the existence

of $Signal \times Signal,\ Signal \times Noise$ and $Noise \times Noise$ terms at the output of the discriminator. Unfortunately, the squaring loss is a complicated expression [2]:

$$S_L = \frac{\mu}{\alpha + \frac{\beta}{4E_s/N_0}}$$

where $\mu$, $\alpha$, and $\beta$ are functions of the correlations of the pulse shape. Therefore, out of convenience, we simulate to estimate (1).

We know that for a square pulse, the variance has a similar structure to (1) [10],

$$\sigma_{2\theta}^{2,\mathrm{squ}} = 4N_{B_L}\left(\frac{1 + 2E_S/N_0}{(E_S/N_0)^2}\right) = 4N_{B_L}\left(\frac{1 + E_{CS}/N_0}{(E_{CS}/2N_0)^2}\right)$$

then

$$\sigma_{\theta}^{2,\mathrm{squ}} = N_{B_L}\left(\frac{1 + 2E_S/N_0}{(E_S/N_0)^2}\right) = N_{B_L}\left(\frac{1 + E_{CS}/N_0}{(E_{CS}/2N_0)^2}\right)$$

where $E_{CS} = 2E_S$ is the energy of a demodulated channel symbol and is due to the Laurent decomposition [2].

From Figure 4, we can see that the variance for $BT_S = 0.5$ and $BT_S = 0.25$ is simply a scaling factor away from square pulse variance for the $E_{CS}/N_0$ simulation range of -5 to 20 dB. Through curve fitting, we find that:

$$\sigma_{\theta}^{2,BT_S=0.5} \approx 0.8N_{B_L}\left(\frac{1 + E_{CS}/N_0}{(E_{CS}/2N_0)^2}\right)$$

and

$$\sigma_{\theta}^{2,BT_S=0.25} \approx 1.3052N_{B_L}\left(\frac{1+E_{CS}/N_0}{(E_{CS}/2N_0)^2}\right).$$

This completes the mathematical model of the baseline architecture, see Figure 3. Note that the symbol *A* refers to the amplitude of the received signal.

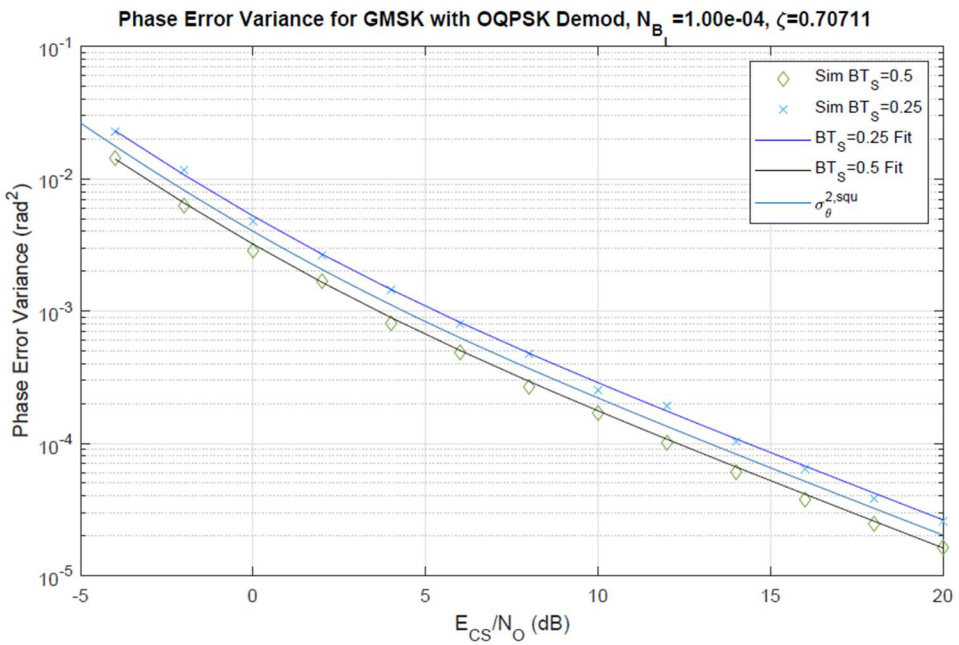


*Figure 4: Variance of Phase Error with Fitted Data Based on $\sigma_\theta^{2,squ}$*

**Cycle slips**

Due to the sinusoidal nature of the S-curve, Figure 2, the stability of the carrier loop when locked around zero phase error can be lost due to noise or changes to the lock point cause by loop stress [6]. A second order loop may reestablish lock multiples of π cycles away. The number of cycles depends on the nature of the phase error as noise, frequency steps and frequency ramps are the most stressful for second order loops.

The mean time to cycle slip (MTCS) was calculated exactly in closed form for 1st order loops by Viterbi [7]. 2nd order loop MTCS analysis was estimated and extended to cover Nth order analysis based on a double integral exponential calculation from Tausworthe [8]. It was later expanded to account for frequency ramps by Lindsey [9]. Our strategy is to perform simulations on the GMSK signal with and without PN and curve fit with no frequency dynamics using this analysis. Once GMSK/PN is fitted, we make predictions on the MTCS performance with a frequency ramp specified by a normalized frequency ramp $\gamma = \text{frequency ramp} \times 2\pi/\omega_n^2$, where the frequency ramp is specified in Hz/sec and $\omega_n$ is the natural frequency of a second order loop in rads/sec$^2$. This semi-analytical approach has made good predictions of higher SNR simulation points that took months of execution time to verify.

**Results and Analysis**

For the case of $BT_S = 0.5$, we set the normalized loop BW $N_{B_L}$=2.5e-3 in Figure 5 and simulate with the baseline architecture without the PN interferer. The curve fit is very tight with the simulation results and so we conclude that the approach very sound.

In Figure 6, we assess the impact of the PN as an interferer, we set the PN modulation index to 0.444 using the T4B sequence, a sine waveform and record the loss. The results show that an SNR loss of 0.76 dB in the prediction matches the simulation data.

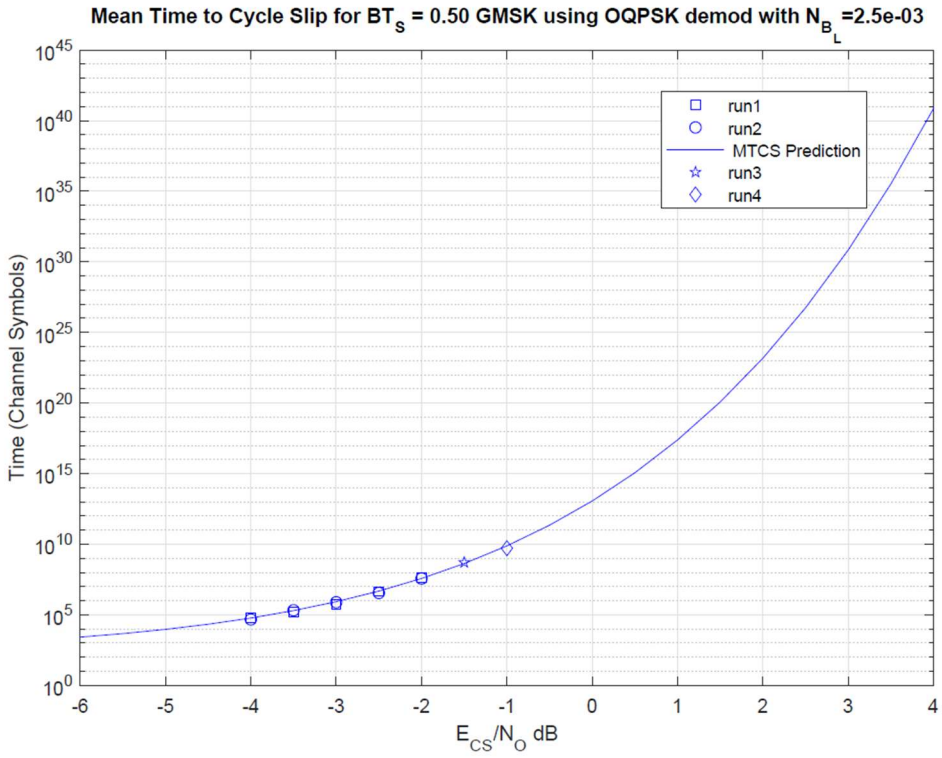


*Figure 5: MTCS for $BT_S = 0.5$*

We now assess the dynamic compensation capability of the baseline architecture when signal is distorted with a frequency ramp. FFigure 7 shows the MTCS prediction with a frequency ramp of $\gamma = 0.01, 0.05, 0.1, 0.2, \text{and } 0.3$. As the results show, the prediction tracks each ramp with good accuracy up to $\gamma = 0.1$, diverges at $0.2$ slightly and more significantly at $0.3$. This could be because of differences between discrete time implementation and the continuous differential equation model or the additional memory effects in the loop which gets more pronounced as $\gamma \to \frac{1}{2}$. Also, when $\gamma = 0.4, 0.5$ the prediction fails which is consistent with the simulations failures as well. Recall that for a second order squaring loop, there is a limit of $\gamma = \frac{1}{2}$ predicted from the linear model that is consistent with our prediction. Note that as $\gamma \to \frac{1}{2}$, floors occur at lower $E_S/N_0$ which is due to false locking after a cycle slip as indicated in the circled areas and will result in receiver failure. This phenomenon is discussed in [6].

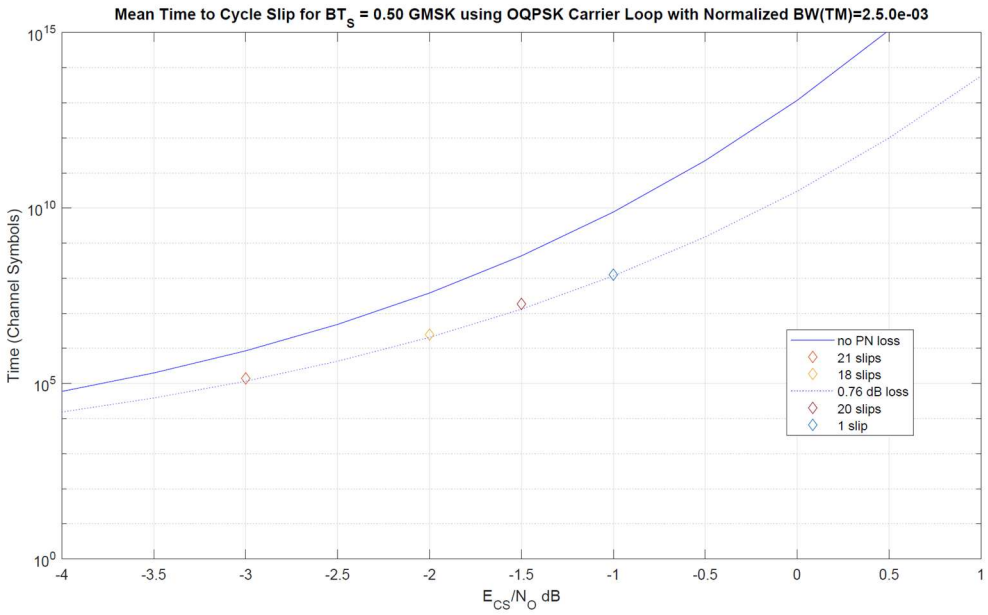


*Figure 6: Impact of PN interferer with Mod Index 0.444*

Figure 8 shows the performance of $BT_S = 0.25$. We can see here that performance is much worse than $BT_S = 0.5$. In fact, the MTCS tends to hit a floor at $\gamma > 0.01$ compared to $BT_S = 0.5$ where at $\gamma > 0.3$ it becomes inoperable. And therefore, the difference between $BT_S = 0.5$ and $BT_S = 0.25$ is an order of magnitude difference in normalized frequency ramp.

To increase the frequency ramp performance of $BT_S = 0.25$, we consider the optional architecture, i.e., moving the derotator in front of the matched filter. The performance is shown at Figure 8 for $\gamma = 0.01$. We can see that there is a slight improvement in the MTCS, i.e., a factor of 2 gain at $E_{CS}/N_0$=1 dB, which leads us to conclude that some improvement can be gained with architecture. However, it was still not possible to operate $\gamma > 0.01$.

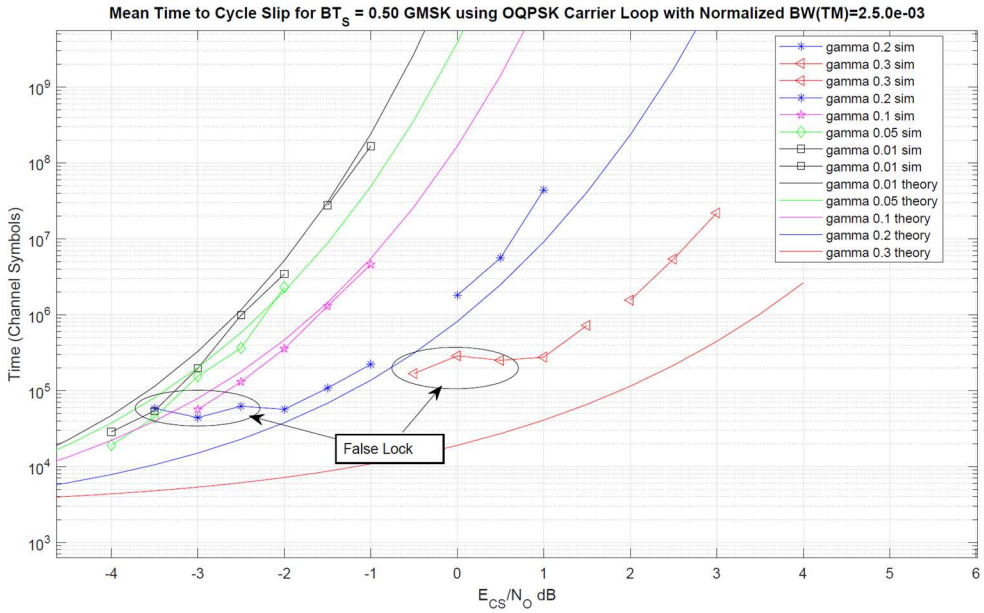


*Figure 7: Baseline Architecture with Various Frequency Ramps*

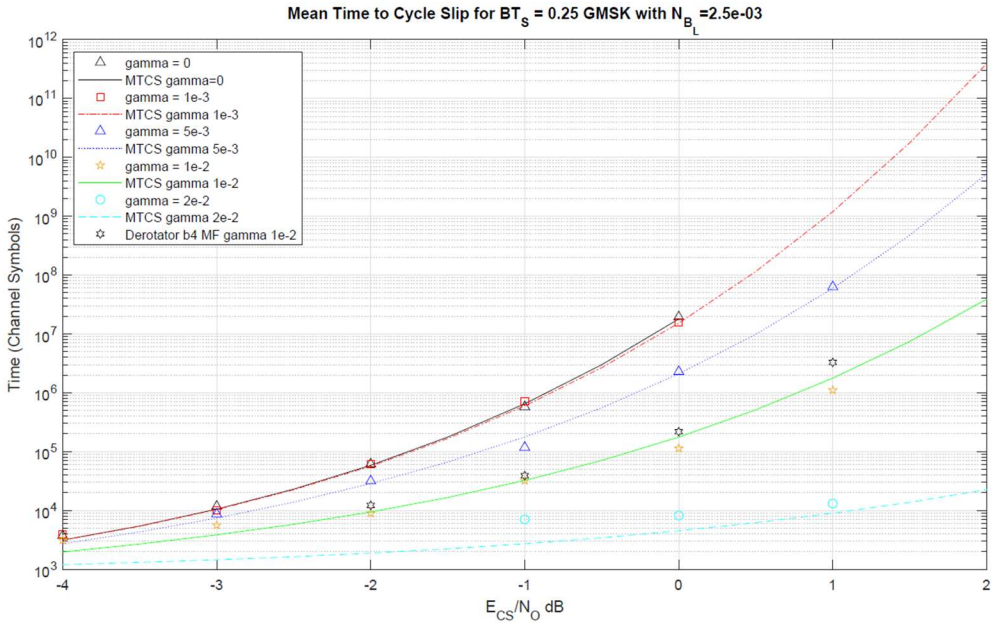


*Figure 8: $BT_S = 0.25$ MTCS Performance*

**Hardware validation**

Some effort was performed to validate the $BT_S = 0.25$ MTCS performance with actual hardware for $N_{B_L} = 2.5e-3$, see Annex **Reliable carrier phase synchronization with GMSK+PN - configuration aspects** Table 3. The $\gamma = 0.02$ inoperability threshold was confirmed. We must

caution that this conclusion has a caveat. The architecture of the hardware is not identical to low-SNR MAP used in this analysis. It is more related to the high-SNR MAP [10]. The fact that both architectures arrive at the same inoperable point leads one to conclude that the result is fundamental. However, further hardware testing of other modes appears to exceed this threshold using a much smaller $N_{B_L}$, see Annex **Reliable carrier phase synchronization with GMSK+PN - configuration aspects** Table 4. We call these modes exceptional modes and simulated these conditions as best as we can, given the hardware and software limitations. The following section describe the analysis and results.

**Testing of exceptional modes**

Mode C4 from Annex **Reliable carrier phase synchronization with GMSK+PN - configuration aspects** Table 4 has the largest $N_{B_L}$ listed in the table. Therefore, we target this mode for analysis. The $N_{B_L} = 5.83e-4$ and the $\gamma = 0.198$. Due to memory limitations, the initial evaluation had a simulation time limited to 8 seconds. Results indicate there is a static phase error caused by the frequency ramp (and directly related to $\gamma$) that will linearly drift upward until it reaches around $\frac{\pi}{2}$ and slips. The assumption is that the system is essentially noiseless due to the small $N_{B_L}$ and if you apply too high of frequency ramp (possibly due to exceeding $\gamma = 0.02$ or pull-in time is too great), the loop cannot reacquire and therefore can no longer track the frequency ramp and a reset must occur. This catastrophic failure is predictable; however, in real operations, it would depend on the spacecraft path and the accumulated phase error. Figure 9 shows the entire run and the point is reached at around 7.5 seconds that the phase error will grow unbounded which indicates that a catastrophic failure has occurred. In Figure 10, we show a close-up of the event that at a phase error of around $\pi/2$, the failure starts and grows unbounded. Both figures show the output of the control loop filter and the prediction if the loop was tracking a frequency ramp properly.

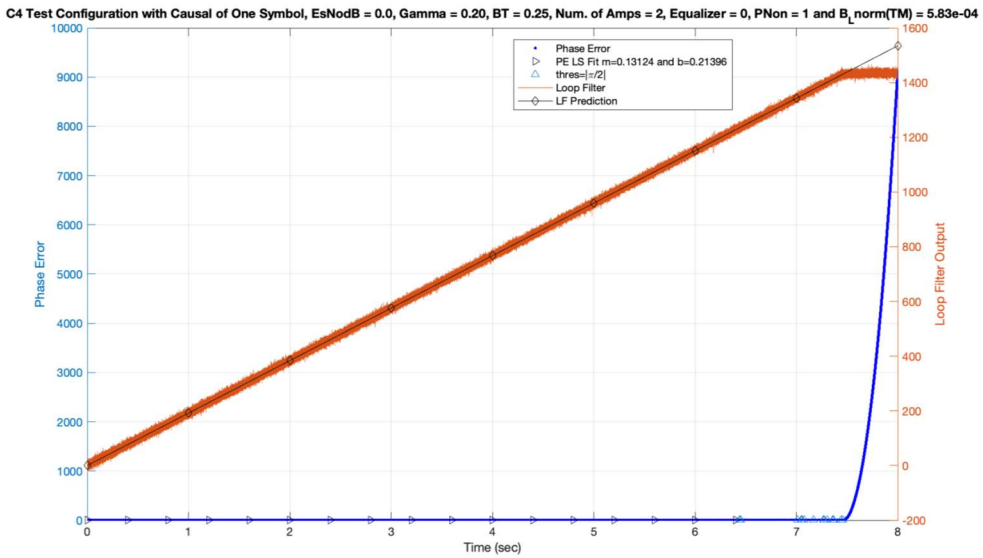


*Figure 9: C4 Scenario with MAP sync and one symbol causal delay*

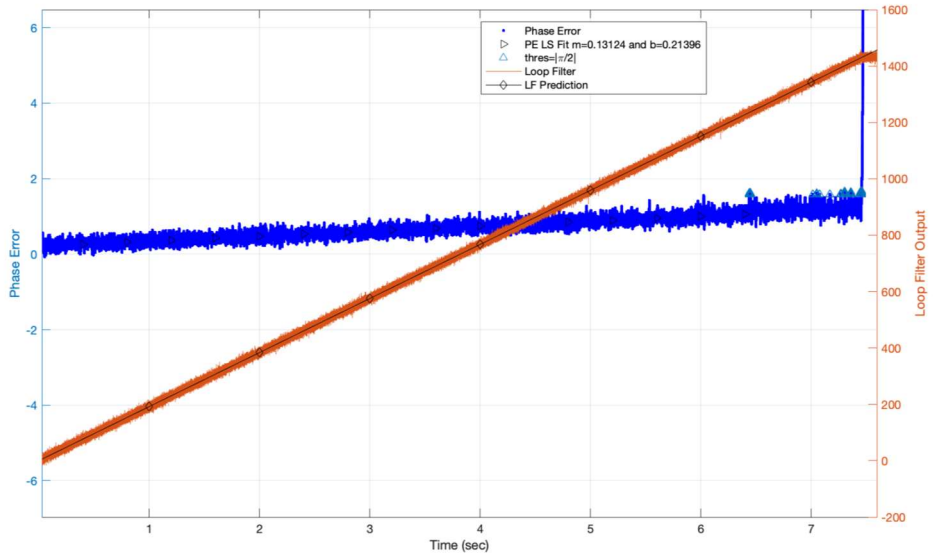


*Figure 10: Zoomed in plot of Figure 9*

When we reduce $\gamma = 0.01$, the deterministic phase error growth no longer exists and the failure goes away, see Figure 11.

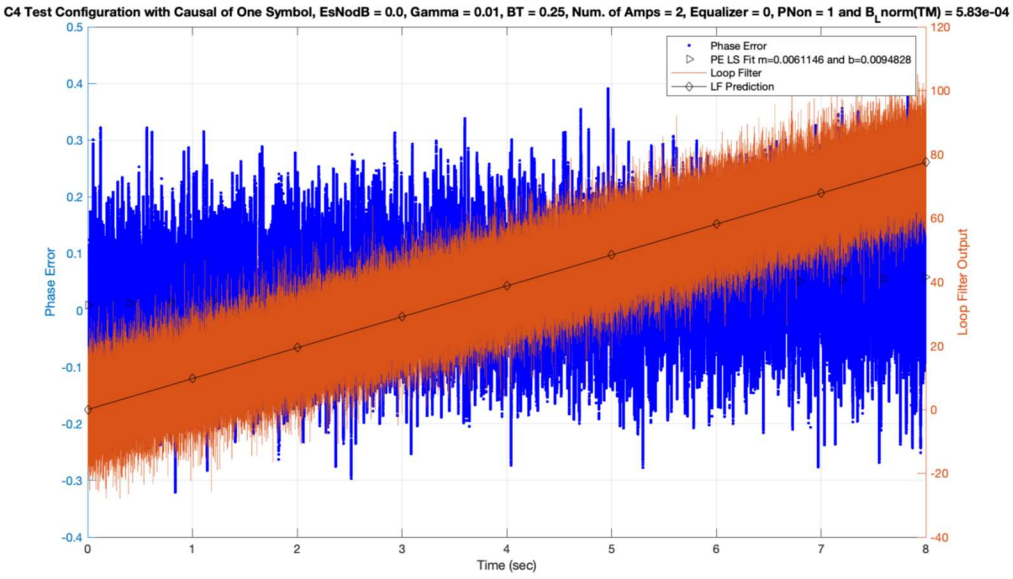


*Figure 11: γ reduced to 0.01*

Our conclusion here is that delays from the loop will create a non-static phase error which will increase linearly with predictable time that will produce a catastrophic slip. Note that the above results from Figures 9-11 were performed with the baseline architecture. We attempted to use the optional architecture as well, but this was found to be ineffective. Therefore, we try to focus on minimizing the

delays in the loop and they were two-fold: 1) delay from matched filter and 2) delay from causality in loop. A causality delay is required for any discrete feedback loop. The matched filter delay cannot be changed, therefore we looked to minimize causality delay. Our MAP architecture implemented a single symbol delay to be in line with decimation to one sample per symbol. As a possible reduction in the delay, we can instead implement a single sample delay which would reduce the causality by a fraction of a symbol, the actual value depends on the number of samples per symbol. Figure 12 shows the simulation under these conditions. Note that the determistic failure has been mitigated. We also ran the simulation with the equalizer on (see Figure 13) and the results were the same.

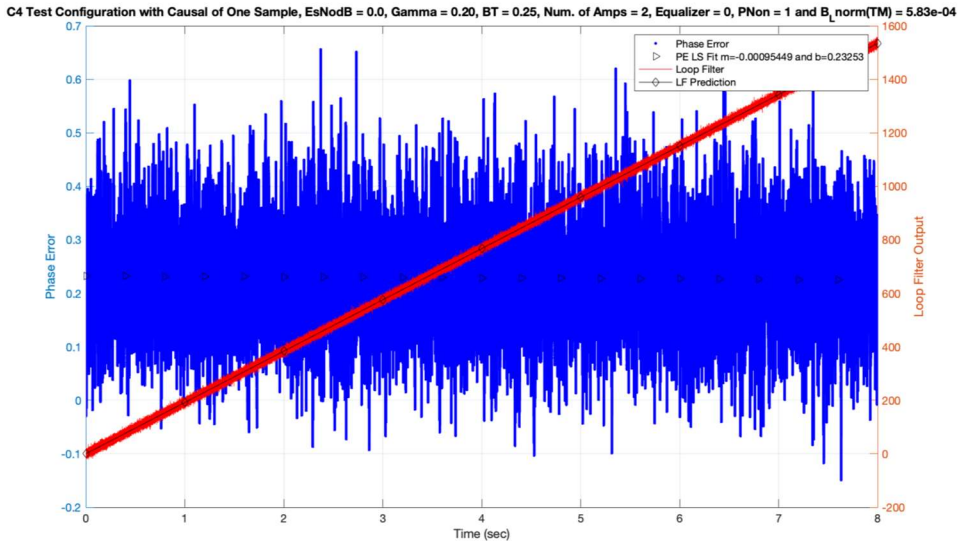


*Figure 12: One Sample Causal Delay MAP Sync for 8 Seconds*

We now increased $\gamma = 0.3$ and ran the simulation again and observed a random catastrophic failure (see Figure 14). Compared to the single symbol delay circuit, it's likely that the single sample delay circuit is an improvement because you removed the deterministic catastrophic failure, however, results indicate that a probabilistic failure around 2.4 seconds will create the same catastrophic failure as a symbol delay circuit**.**

We tried different settings for mode C4 using: 1. PN square pulse and 2. $BT_S = 0.5$. What we found was that a square PN pulse has no ability to track any of the γ settings we used. And $BT_S = 0.5$ shows similar behavior.

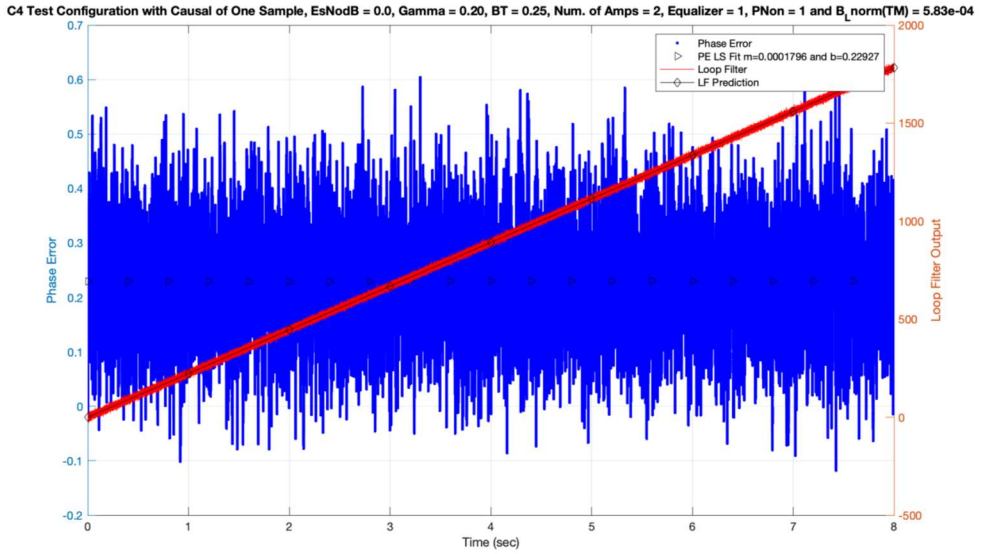


*Figure 13: One Sample Causal Delay MAP Sync with Equalizer On*

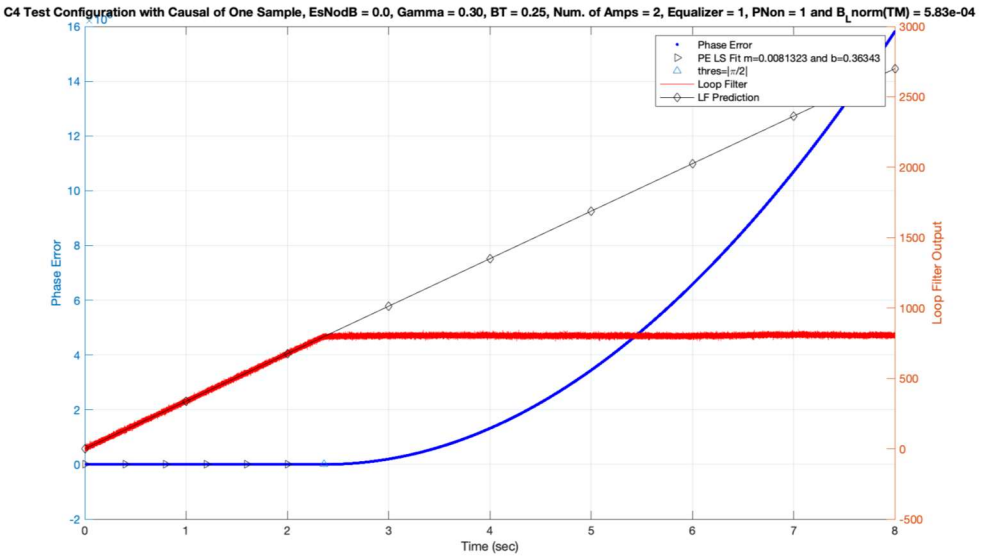


*Figure 14: Gamma set to 0.3 on Second Run and Observed a Random Catastrophic Failure*

**Conclusion**

We have mathematically modelled the low-SNR MAP carrier lock successfully using a semi-analytical approach where we curve fit simulation data of GMSK/PN and then use a mathematical formula to estimate its performance with a frequency ramp. $BT_S = 0.5$ demonstrated robustness to normalized ramp of $\gamma \leq 0.3$ using $N_{B_L} = 2.5e-3$, however, $BT_S = 0.25$ showed an order of magnitude loss in

performance, i.e., $\gamma \leq 0.01$. We tried to mitigate this loss by using the optional architecture. However, we were not successful. Hardware testing confirmed the $\gamma = 0.02$ inoperability point for this case scenario. Subsequent testing using smaller $N_{B_L}$ settings allowed higher values of $\gamma$, however, when we analyzed the C4 scenario catastrophic failures occurred.

We showed that delays can cause catastrophic deterministic sync failures in MAP synchronization circuits. A new single sample delay sync design over the previous single symbol sync design was considered. This demonstrated that it may be possible that deterministic sync failures shown in C4 scenario with symbol delay loops can be mitigated with a sample delay loop. However, we cannot conclusively say this is an improvement since we can't do an MTCS analysis for $N_{B_L}$ so low. We have also shown that if we further take $\gamma = 0.3$ in C4 scenario with a sample delay loop, it will randomly produce catastrophic failures. The static phase error worsens as an increasing function of $\gamma$. Also that if you keep $\gamma < 0.02$, the tilt in the phase error goes away in symbol delay loop. Since we are constrained by computer memory, we cannot assess the MTCS for the C4 scenario. Given that we cannot fully validate C4, we would not recommend using the $\gamma = 0.198$ setting. However, should the implementer choose to use the C4 scenario with a high value of $\gamma \geq 0.02$, they should do extensive testing to ensure that occurrence of random catastrophic failures do not significantly reduce the mission link availability requirement. As a conservative design strategy, setting $\gamma < 0.02$ will produce a robust system according to the simulations and analysis for both $BT_S = 0.5$ and $BT_S = 0.25$. If systems need to reach higher frequency ramp tolerance, $BT_S = 0.5$ with $N_{B_L} = 2.5e-3$ was shown to be robust to frequency ramps of $\gamma < 0.2$ with some false locking at lower SNRs with $\gamma = 0.2, 0.3$.

REFERENCES


[1] *Bandwidth Efficient Modulations—Summary of Definition, Implementation, and Performance*. Informational Report (Green Book), CCSDS 413.0-G-3. Washington, D.C.: CCSDS, February 2018.

[2] M. Simon, *Bandwidth-Efficient Digital Modulation with Application to Deep-Space Communications*, Descanso, 2001.

[3] M. Jeruchim, P. Balaban, and K. Shanmugan, *Simulation of Communication Systems: Modeling, Methodology and Techniques 2nd. Ed.*, Kluwer Academic, New York, NY, 2000.

[4] W. Fong and W. Lee, "SLS-RFM 17-07: NASA/GSFC Report on CCSDS Recommendation 2.1.8A/B Minimum Earth Station Transmitter Frequency Resolution for Spacecraft Receiver Acquisition", *CCSDS Radio-Frequency and Modulation Spring 2017 Meeting, San Antonio, TX*, April 3, 2017. http://hdl.handle.net/2060/20170004526

[5] U. Mengali and A. D'Andrea, *Synchronization Techniques for Digital Receivers*, Springer, New York, NY, 1997.

[6] F. Gardner, *Phaselock Techniques, 3rd Ed*., John Wiley and Sons, Hoboken, NJ, 2005.

[7] A. Viterbi, *Principles of Coherent Communications*. McGraw-Hill, New York, NY, 1966.

[8] R. Tausworthe, "Cycle Slippage in Phase-Locked Loops," *IEEE Transactions on Communication Technology*, Vol. 15, No. 3, June 1967, pp. 417-421.

[9] W. Lindsey, *Synchronization Systems, In Communication and Control*, Prentice Hall, Englewood Cliffs, NJ, 1972.

[10] M. Simon, “Carrier Synchronization of Offset Quadrature Phase-Shift Keying”, Telecommunications and Mission Operations Progress Report, TMO 42-133, May 15, 1998, pp.1-33. https://pdfs.semanticscholar.org/5985/aec8cdd7f93a285f01d0d8d9a71be7b0bf25.pdf