National Aeronautics and Space Administration

Phase Noise Study for Cross Links

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October 18-20, 2022

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Background

- This study is the response to RFM Action AI_22-04: Review the 22 GHz phase noise mask in the proposed Recommendation 2.2.10, and comment on its applicability for use in the draft Recommendation 2.4.25.
- We analyze the potential of updating the proposed phase noise mask to Rec. 2.2.10 for crosslinks.
- We are following the proposed draft recommendation 2.4.25 for minimum data rate and band specification for recommends (1).
- We are assuming that the current CCSDS mask is the received phase noise mask.
- We attempt to answer the question: is it necessary to include additional considerations to the current CCSDS mask?

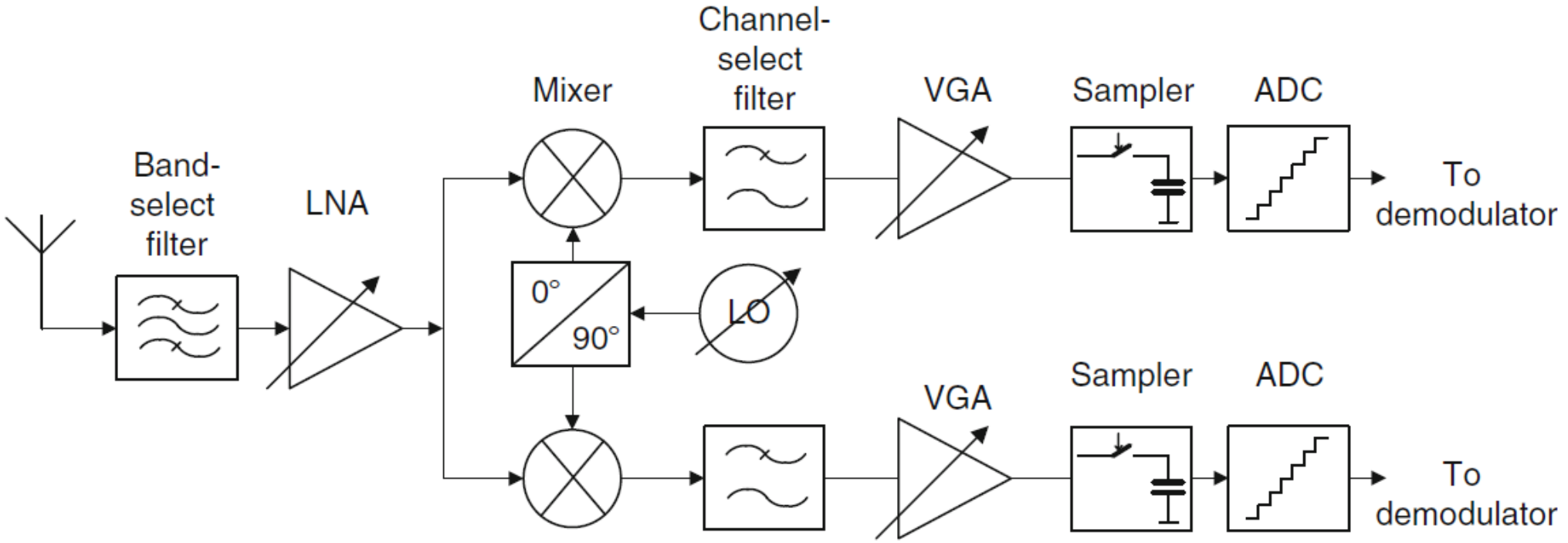
Plan of Attack

- We look at three receiver architectures and select the worst-case phase noise profiles.
- We follow a semi-analytical approach using linear theory to create phase noise profiles and then use the profiles as inputs into a simulation model.
- We take a careful look at total phase noise profile into the demodulator also using the clock phase noise profile as VCO phase noise.
- We simulate the demodulator and find the BER with a full phase noise breakdown and compare that to the case of an ideal receiver with only the CCSDS phase noise mask as input.

Three Popular Receiver Architectures

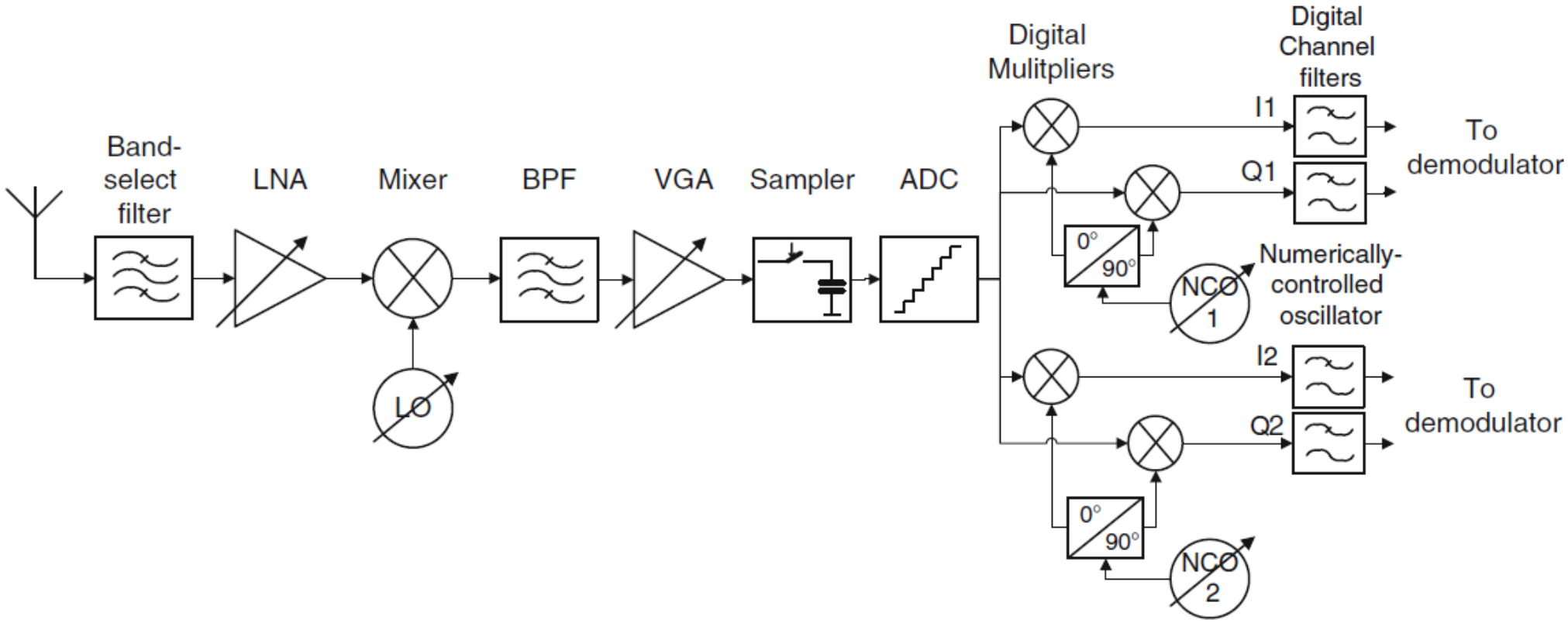
- Direct Conversion
- Digital IF
- Super-Heterodyne

Direct Conversion



Source: Jamin – Broadband Direct RF Digitization Receivers

Digital IF



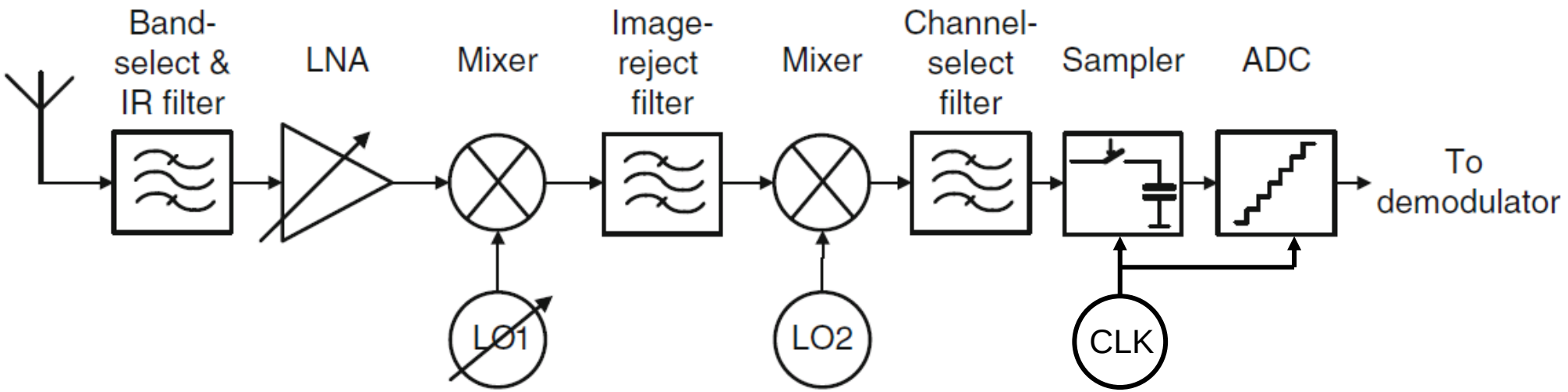
Source: Jamin – Broadband Direct RF Digitization Receivers

Super-Heterodyne

27.5 - 25.25 GHz
> 10 Ms/s

IF1= 1.25 GHz

IF2=70 MHz

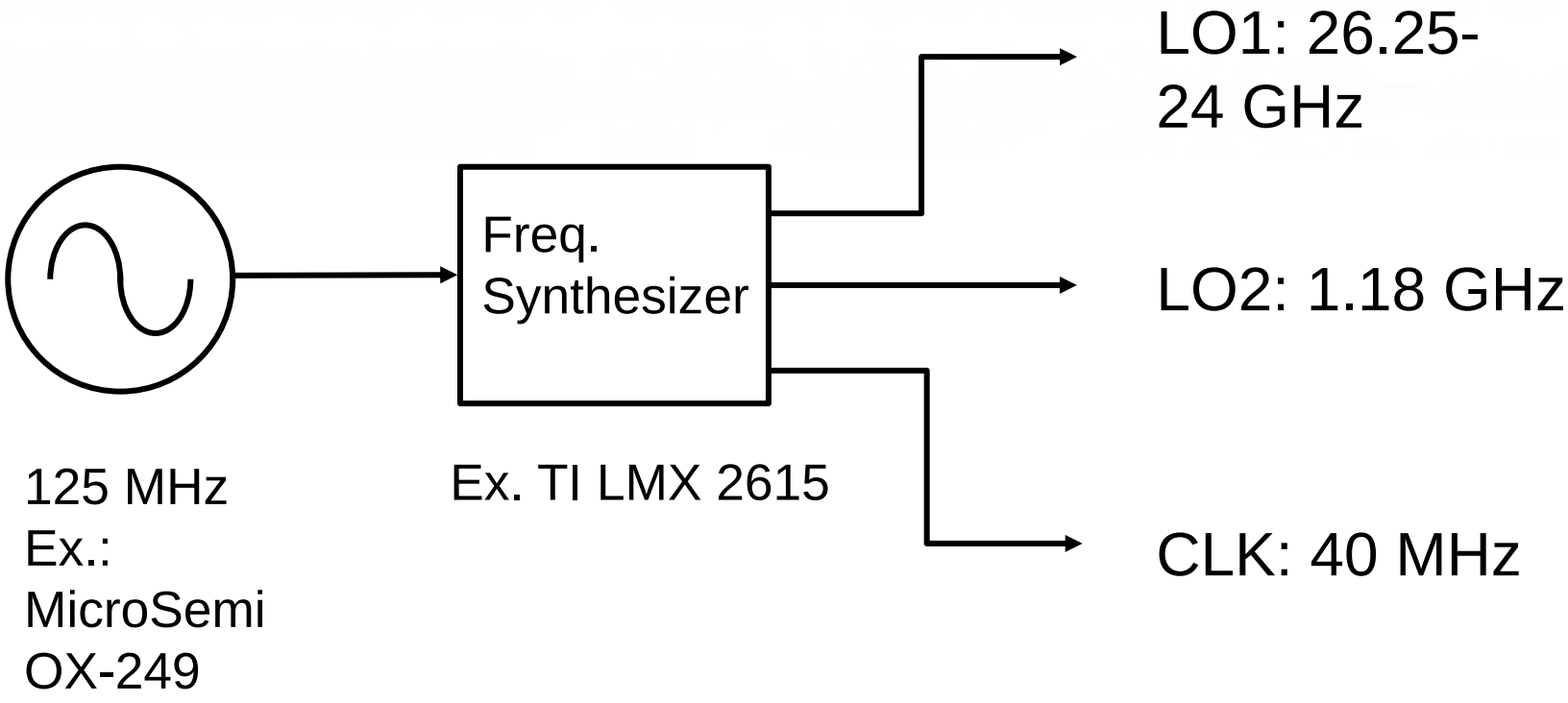


Source: Jamin – Broadband Direct RF Digitization Receivers

Semi-Analytical Plan

- We conclude that the Super Heterodyne is the worst-case receiver because of two levels of heterodynes which adds two phase noise profiles to the input mask
- Therefore, we define the following tasks:
  - Develop Phase Noise Profiles (Masks) of all local oscillators and clock
    - Profiles are based on linear theory of Phase Locked Loops
  - Sum the constituent profiles at every heterodyne stage
    - Total Phase Noise Profile at the input to carrier recovery loop is the summation of CCSDS + LO1 + LO2 phase noise masks
    - Use Phase Noise Clk Profile as NCO phase noise to build a more realistic model
  - With Input Phase Noise Profile and NCO Phase Noise profile defined, simulate GMSK and SRRC-OQPSK demodulator and compute BER using MAP carrier sync.
  - Compare with CCSDS Mask only BER results.

Frequency Distribution Network



Set loop bandwidth to 1e6 Hz.

Phase Noise Brief Review

- Modeled as a stationary process [2].
- Synthesized with a filtered Gaussian Distribution with a specified phase noise profile in PSD defined by dBc/Hz vs Hz
- The output of an oscillator can be defined by: $osc(t) = Asin\big(\omega_0 t + \Delta\phi(t)\big)$, (If amplitude fluctuations and initial phase are zero) where $\Delta\phi(t)$ is the phase noise and ω_0 is the angular frequency.
- Assuming $\Delta\phi(t)$ is small, the single-sided spectrum of the oscillator is: $S_{osc}(\omega - \omega_0) \approx A^2\delta(\omega - \omega_0)/2 + A^2 S_{\Delta\phi}(\omega - \omega_0))/2$.
- Define a spectrum: $L(\Delta\omega) = \frac{2S_{osc}(\Delta\omega)}{A^2} \approx \delta(\Delta\omega) + S_{\Delta\phi}(\Delta\omega)$ where $\Delta\omega = \omega - \omega_0$.
- $S_{\Delta\phi}(\Delta\omega)$ is the phase noise spectrum but $L(\Delta\omega)$ is conventionally used.

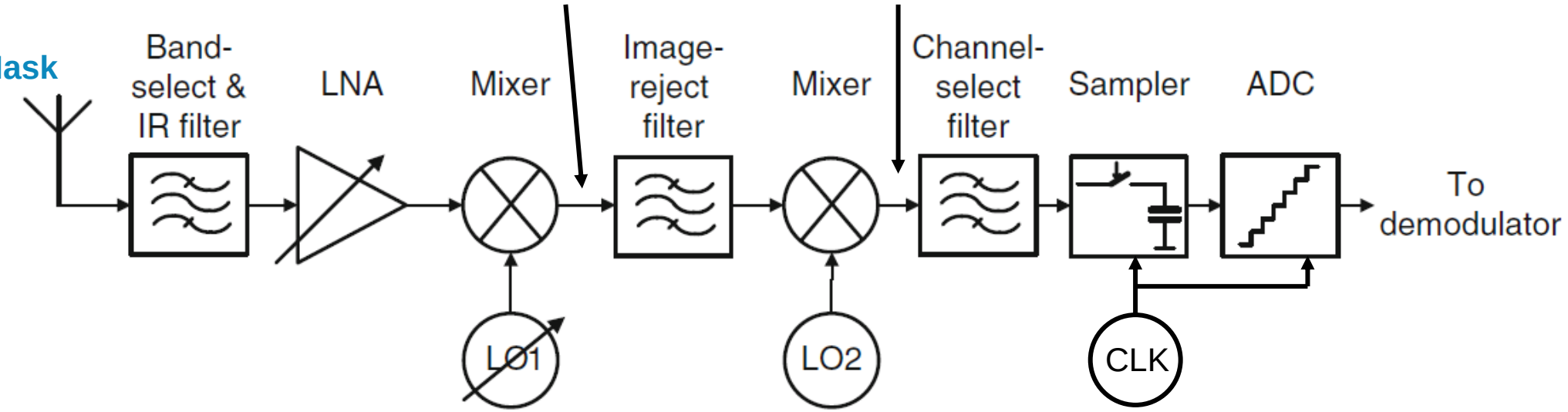
Super-Heterodyne Model

27.5 - 25.25 GHz
> 10 Ms/s

CCSDS Mask

CCSDS Mask + FSP1

CCSDS Mask + FSP1 + FSP2



26.25-24 GHz

Freq Synth
Profile1 (FSP1)

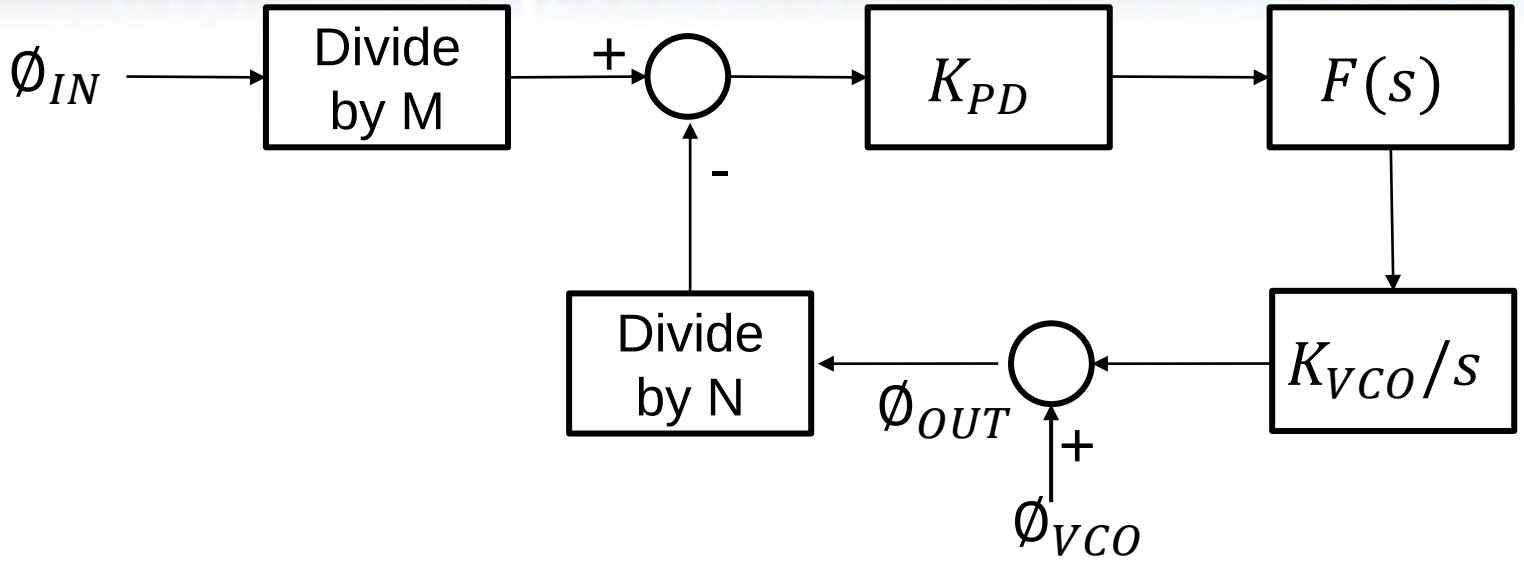
1.18 GHz

Freq Synth
Profile2 (FSP2)

4x10 MHz

Freq Synth Profile3 (FSP3)

Frequency Synthesizer Model



From [1]:

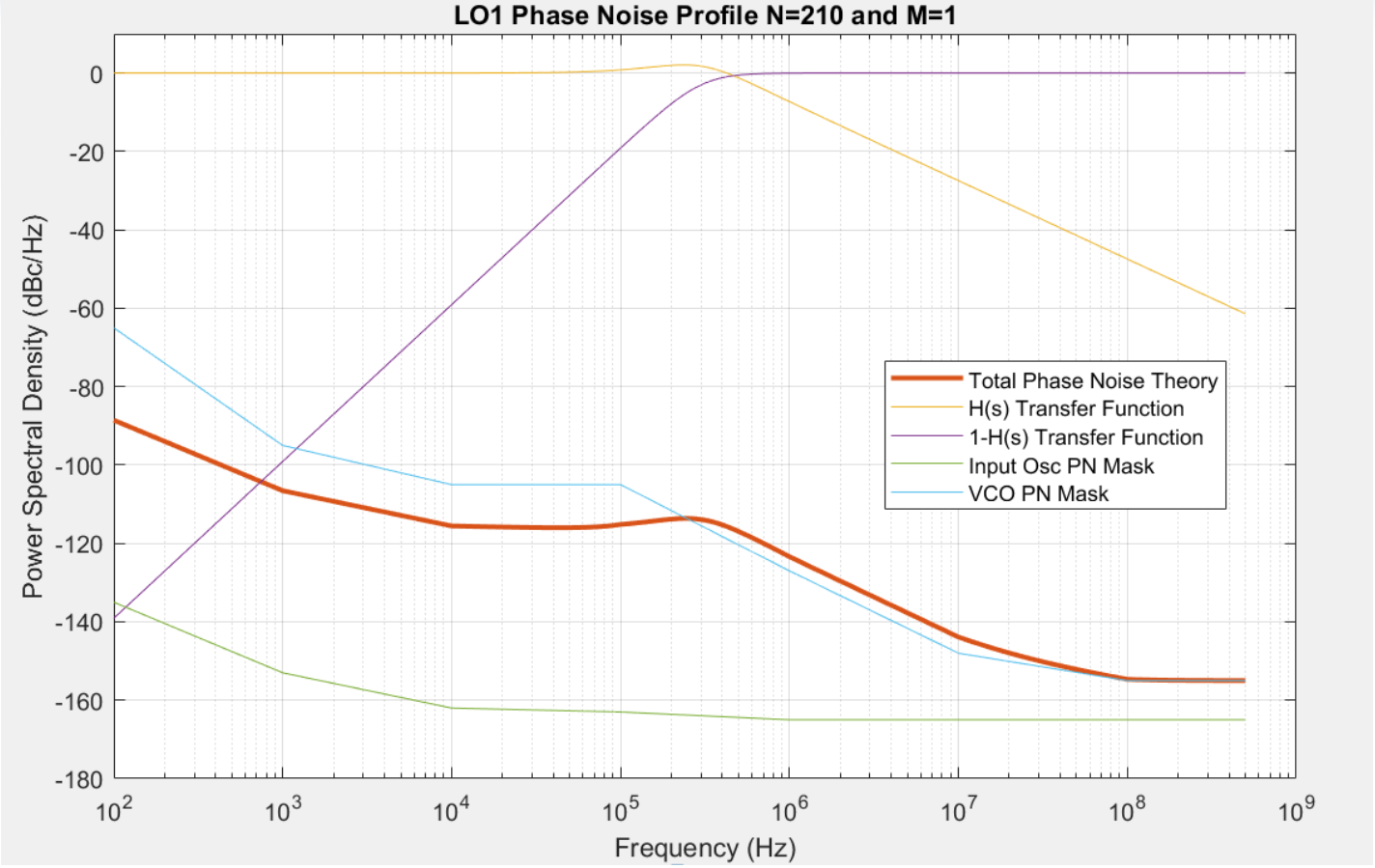
$$\frac{\phi_{OUT}}{\phi_{IN}} = \frac{K_{PD}K_{VCO}F(s)/M}{s + K_{PD}K_{VCO}F(s)/N} = \frac{N}{M}H(s),$$

$$\frac{\phi_{OUT}}{\phi_{VCO}} = \frac{s}{s + K_{PD}K_{VCO}F(s)/N} = 1 - H(s),$$

$$H(s) = \frac{2\xi\omega_n s + {\omega_n}^2}{s^2 + 2\xi\omega_n s + {\omega_n}^2},$$

$$S_{\phi_{OUT}}(f) = \left[\frac{N}{M}\right]^2 |H(f)|^2 S_{\phi_{IN}}(f) + |1 - H(f)|^2 S_{\phi_{VCO}}(f).$$

Frequency Synthesizer Analysis with 26.25 GHz Output Frequency and 125 MHz Input Frequency



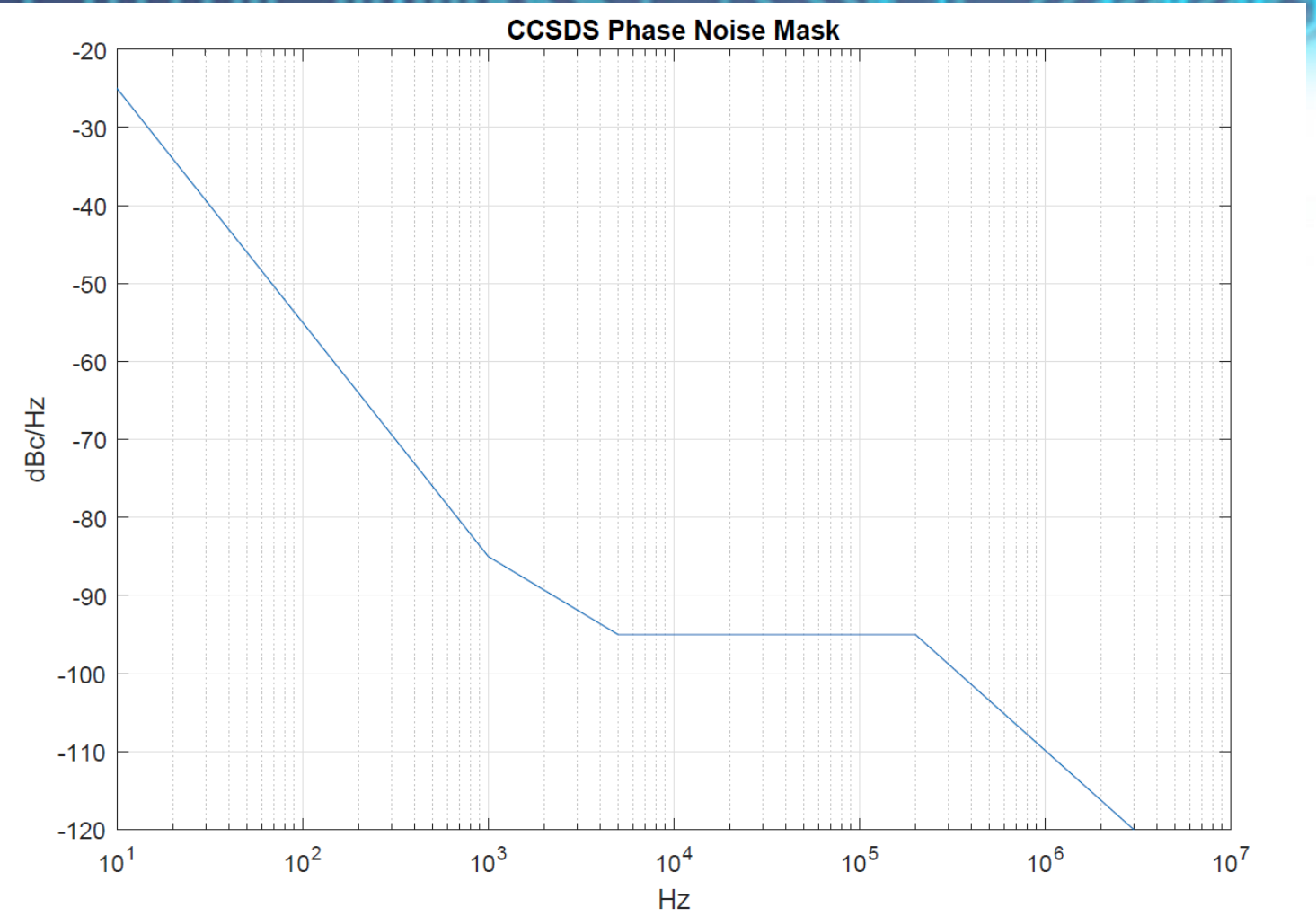
Note: Manufacturer (TI) didn't specify VCO PN mask values below 1e5 Hz, so we made reasonable assumptions. Loop BW = 1e6.

Specific Phase Noise Profiles

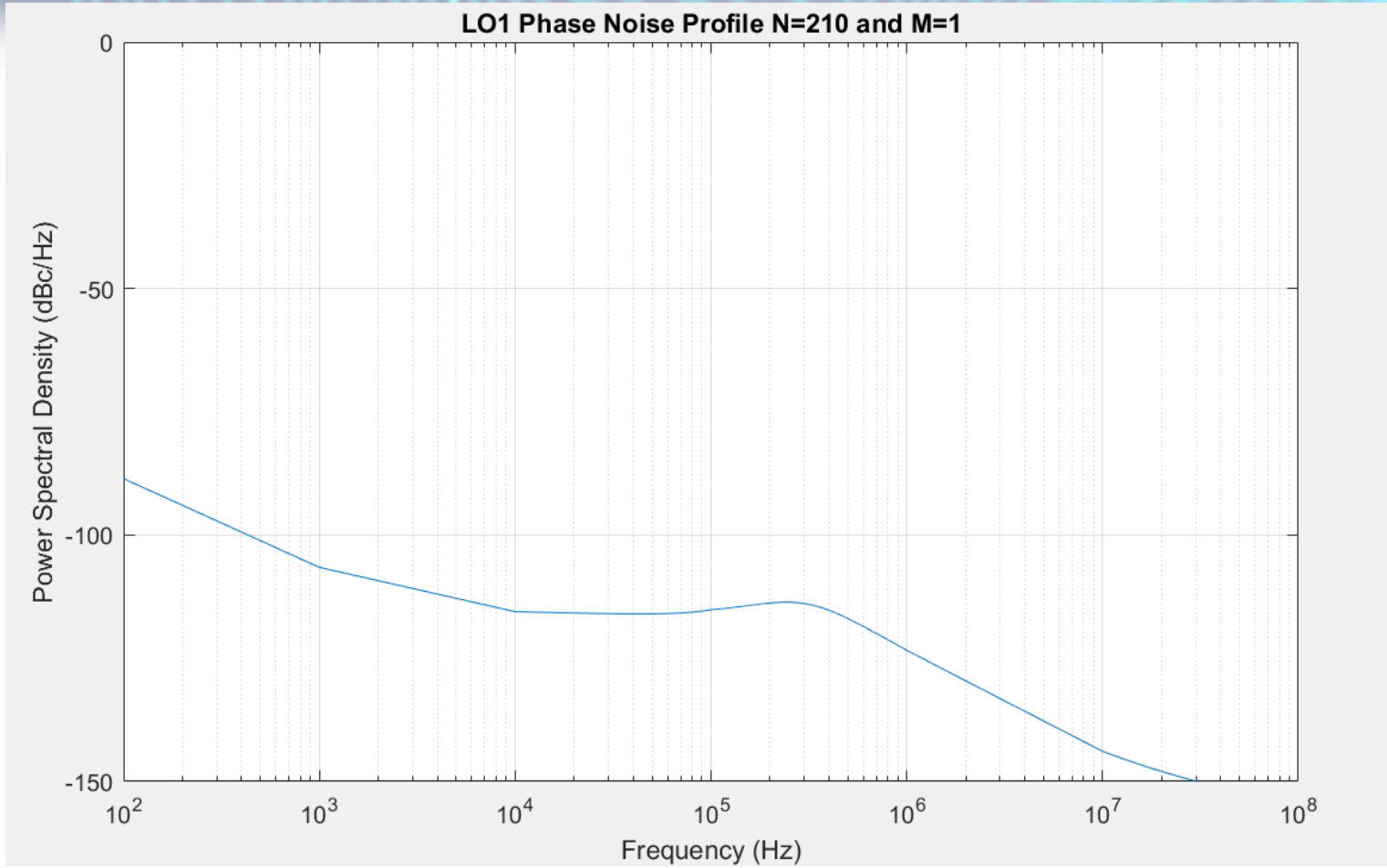
- CCSDS Phase Noise Mask
- LO1 Phase Noise Profile
- Phase Noise Profile at output of Mixer One
- LO2 Phase Noise Profile
- Phase Noise Profile at output of Mixer Two[1]
- CLK Phase Noise Profile[1]

[1]LO1, LO2 and CLK Phase Noises are correlated and profiles could be slightly worse than the prediction.

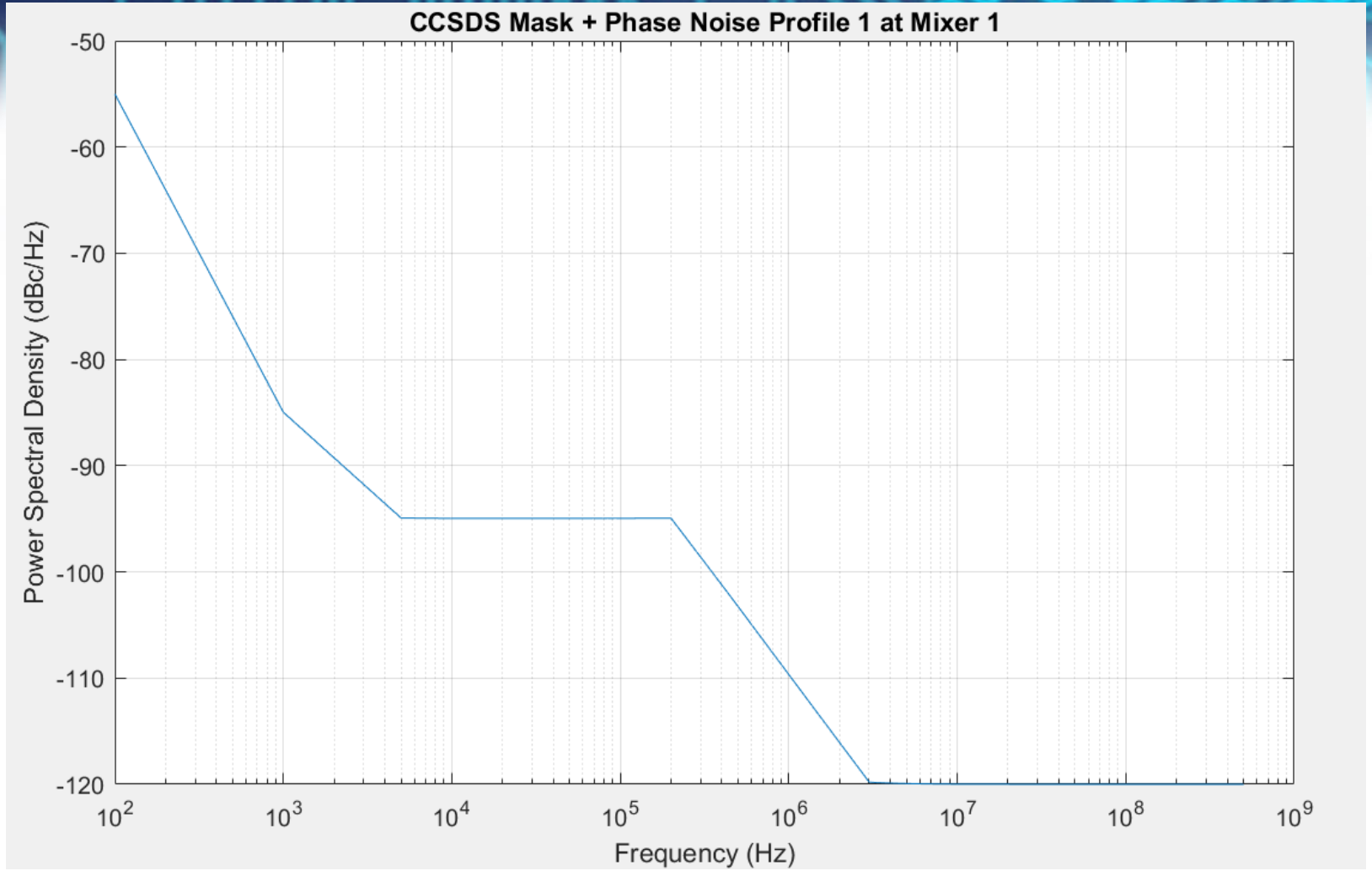
CCSDS Phase Noise Mask



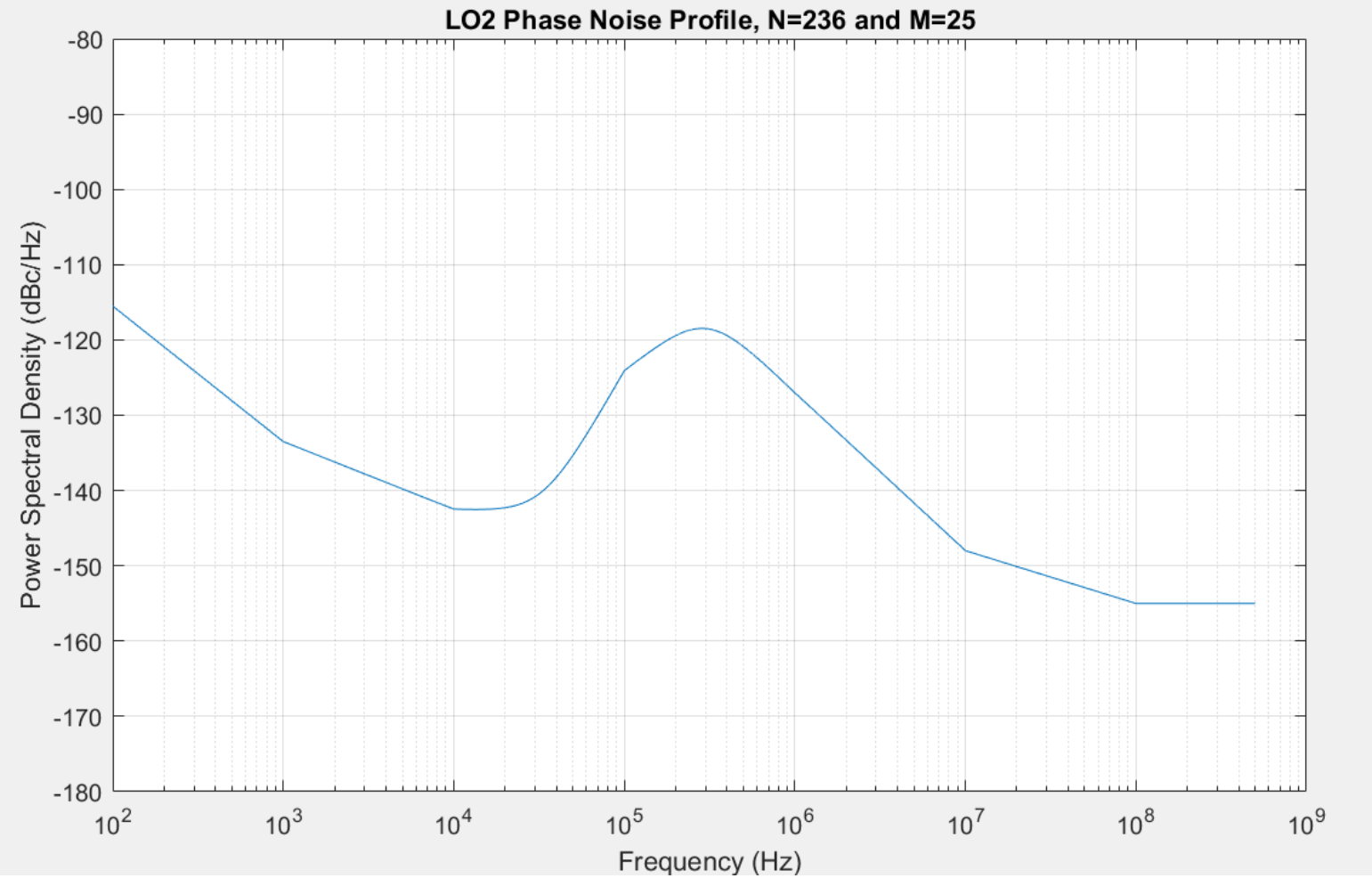
LO1 Phase Noise Profile 26.25 GHz



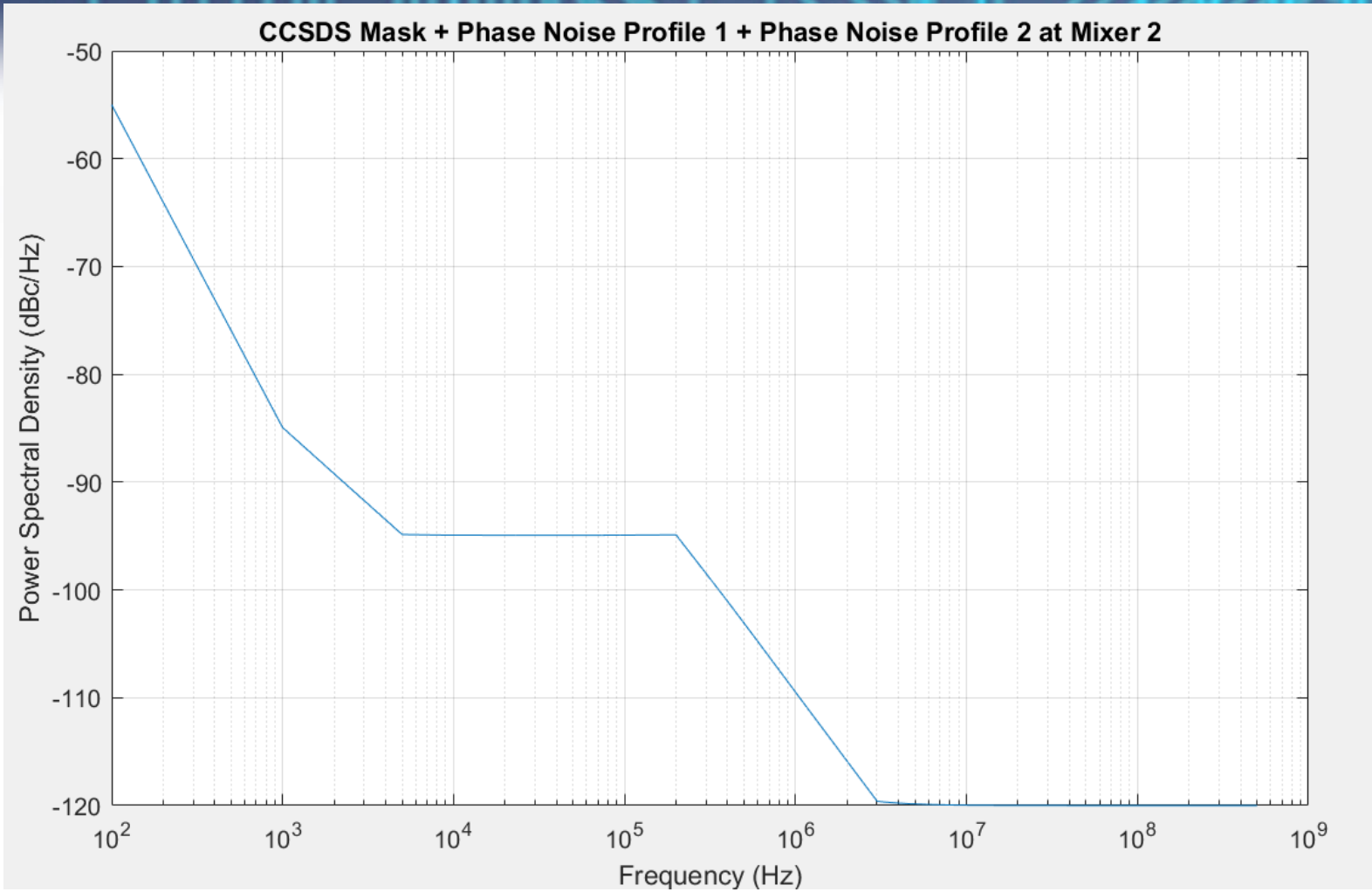
Phase Noise Profile at output of Mixer one



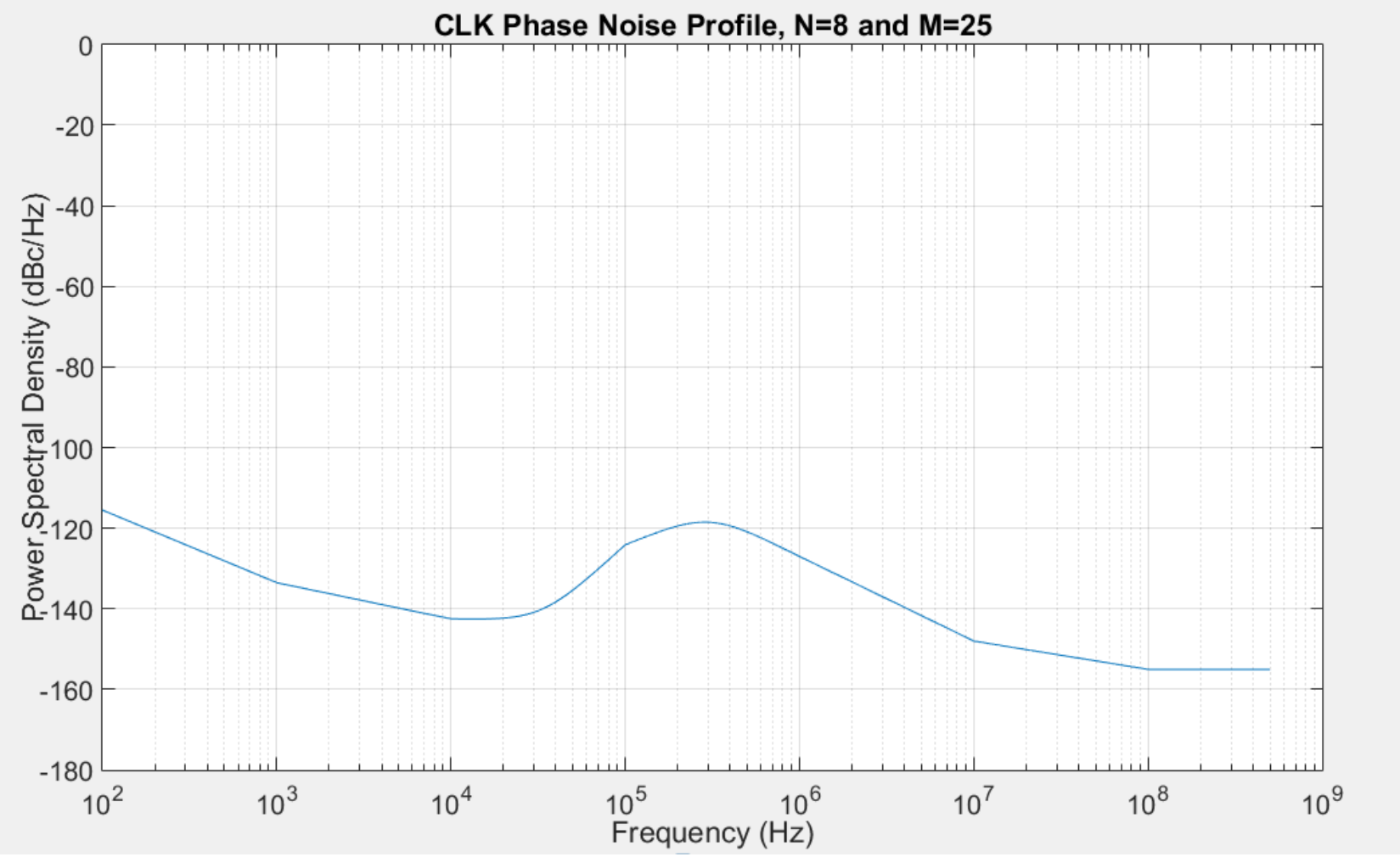
LO2 Phase Noise Profile 1.18 GHz



Phase Noise Profile at output of Mixer two



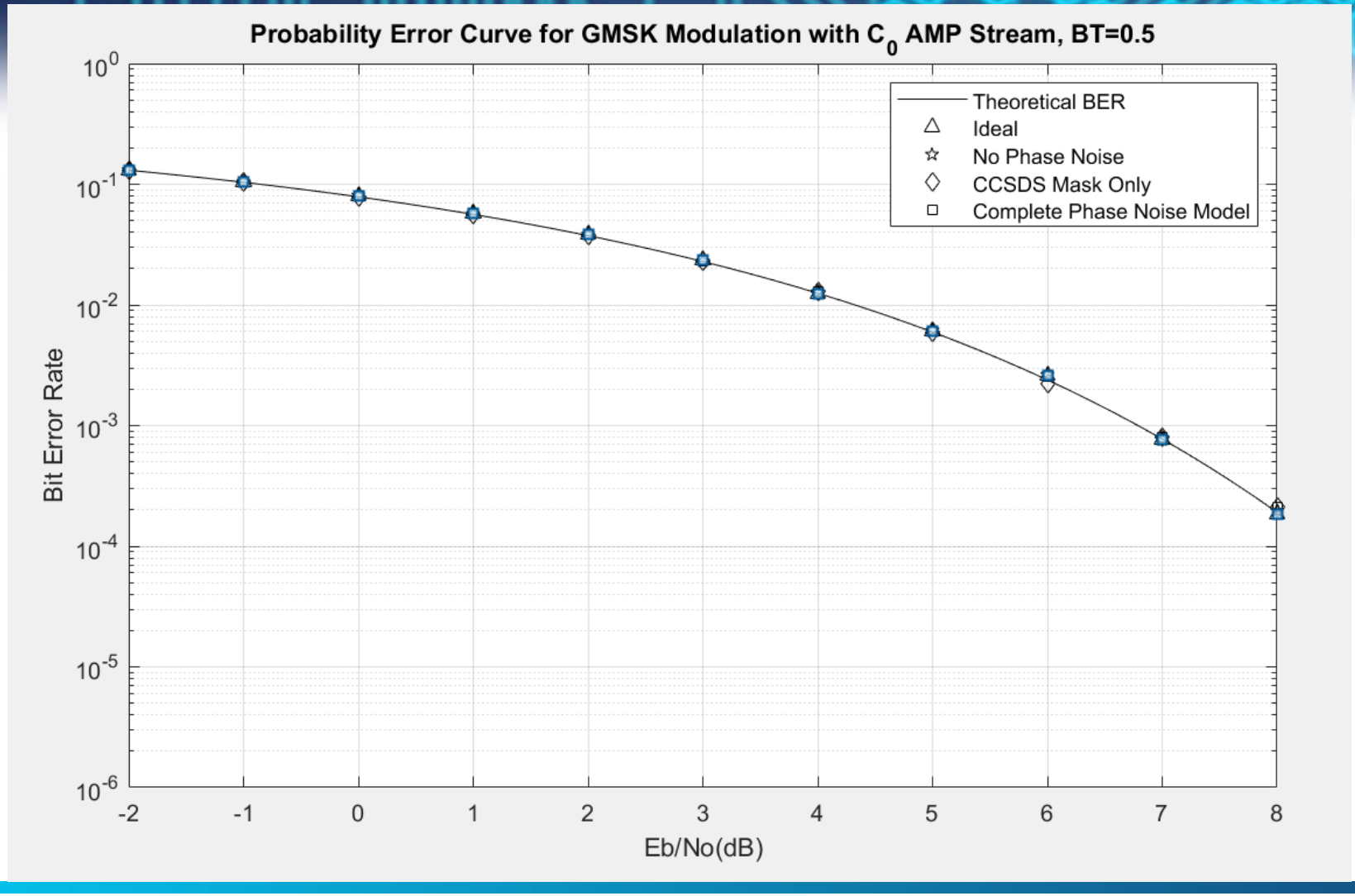
CLK Phase Noise Profile



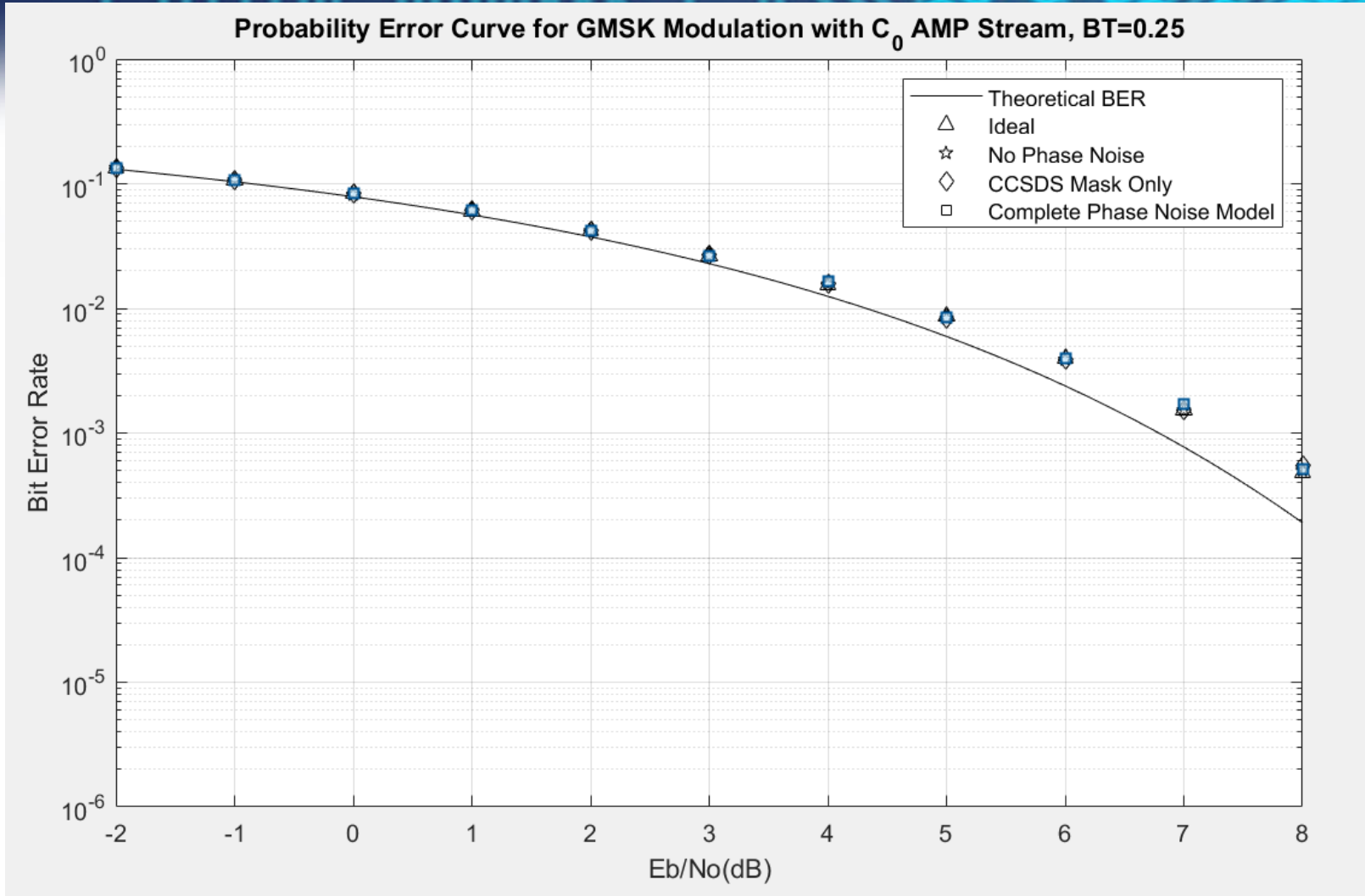
Simulation Results

- Low SNR Implementation of MAP for Carrier Synchronization
- We use a Normalized Loop BW of 5e-4
- Data Rate = 10 Msps
- Zeta=0.7071
- No Equalization for GMSK 0.25

GMSK BT=0.5 BER simulation



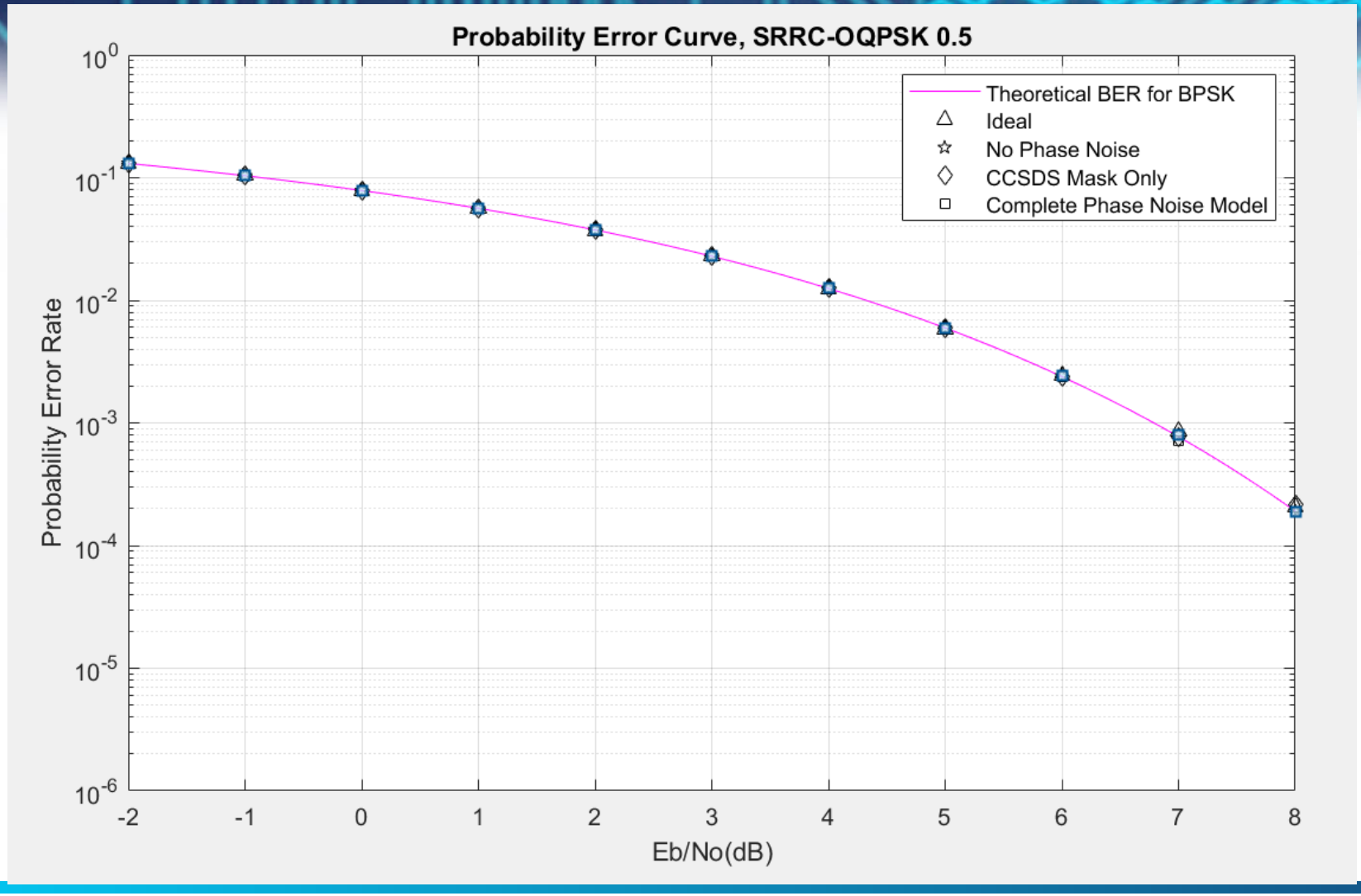
GMSK BT=0.25 BER simulation



GMSK BER Loss Summary with 100 block errors collected from an uncoded block of 2000 bits

GMSK BT=0.5	Rate ½ @ -2 dB Es/No	Rate 7/8 @ 3.4 dB Es/No
Complete Phase Noise Model	NaN dB	7.795e-02 dB
CCSDS Mask Input Only	4.315e-02 dB	6.245e-02 dB
No Phase Noise	4.571e-02 dB	6.745e-02 dB
Ideal	4.147e-03 dB	6.954e-02 dB
GMSK BT=0.25	**Rate ½ @ -2 dB Es/No**	**Rate 7/8 @ 3.4 dB Es/No**
Complete Phase Noise Model	1.174e-01 dB	4.151e-01 dB
CCSDS Mask Input Only	1.436e-01 dB	3.892e-01 dB
No Phase Noise	1.482e-01 dB	3.589e-01 dB
Ideal	6.304e-02 dB	3.480e-01 dB

SRRC-OQPSK 0.5 BER Simulation



SRRC-OQPSK 0.5 BER Loss Summary with 100 block errors collected from an uncoded block of 2000 bits

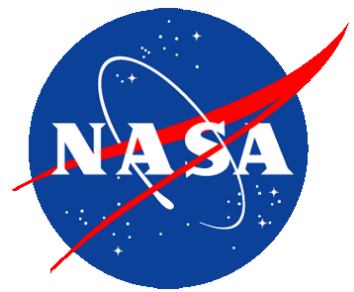
SRRC-OQPSK 0.5	Rate ½ @ -2 dB Es/No	Rate 7/8 @ 3.4 dB Es/No
Complete Phase Noise Model	2.101e-02 dB	6.417e-02 dB
CCSDS Mask Input Only	1.165e-02 dB	5.648e-02 dB
No Phase Noise	1.939e-02 dB	6.421e-02 dB
Ideal	NaN	4.926e-02 dB

Conclusion

- For GMSK 0.5, GMSK 0.25 and SRRC-OQPSK 0.5, the differences between the complete phase noise model, the CCSDS Phase Noise Mask Only, the no phase noise and ideal performances are statistically insignificant.
- We conclude that the additional Phase Noise created by the heterodyning and frequency synthesis is so small that it does not warrant any additional consideration.
- Some consideration can be made to relax the CCSDS Phase Noise Mask, if so, we can extend the work to allow the Phase Noise mask to rise and see when we get significant degradation.

References

- [1] David C. Lee, “Analysis of Jitter in Phase-Locked Loops”, IEEE Transactions on Circuit and Systems—II: Analog and Digital Signal Processing, Vol. 49, No. 11, Nov. 2002
- [2] Francesco Brandonisio and Michael P. Kennedy, *Noise-Shaping All-Digital Phase-Locked Loops*, Springer, 2014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