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CENTRE NATIONAL D'ÉTUDES SPATIALES

LDPC O3K FOR RF

CNES

AIRBUS DEFENCE AND SPACE FRANCE

CCSDS F2F SPRING 2024

1ST OF MAY 2024

SUMMARY

CONTEXT

The SLS – OPT group studied different FEC for the new standard Non coherent optical communication O3K

The need were:

- Encoding and decoding for data rate from 10 Mbps up to 10 Gbps
- Variable useful data rate to cope with varying link budget

Several codes were proposed, based on existing CCSDS RF codes and new ones:

- RF FEC: Turbo/LDPC codes from 131.0 B 3
- RF FEC: SCCC codes from 131.2 B 1
- RF FEC: REED-SOLOMON from 131.0 B 3
- From optical terrestrial network: RS product codes RS(253,221)xRS(248,230)
- New LDPC family proposed by ADS/CNES

The solutions were compared in terms of performances and implementation complexity

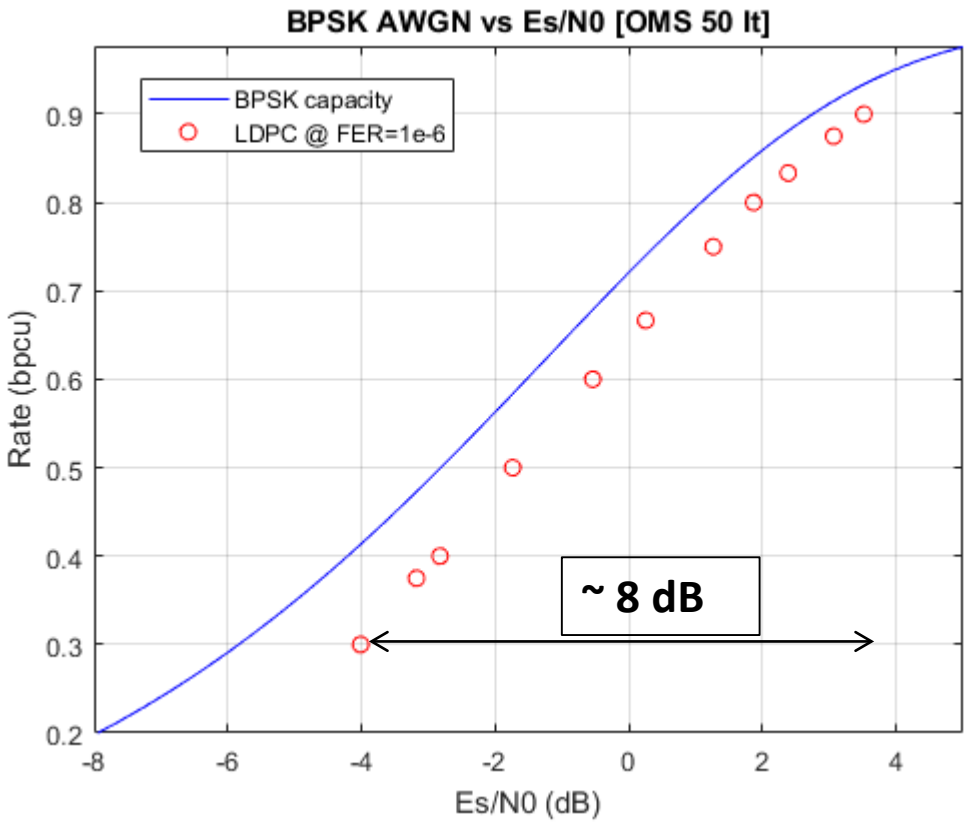
Two codes were selected for O3K:

- REED-SOLOMON from 131.0 B 3
- The new LDPC family with code rates ½ and 9/10, and spread spectrum technique

1. CCSDS O3K LDPC MOTIVATIONS

Purpose → to provide a family of FEC codes with the following features:

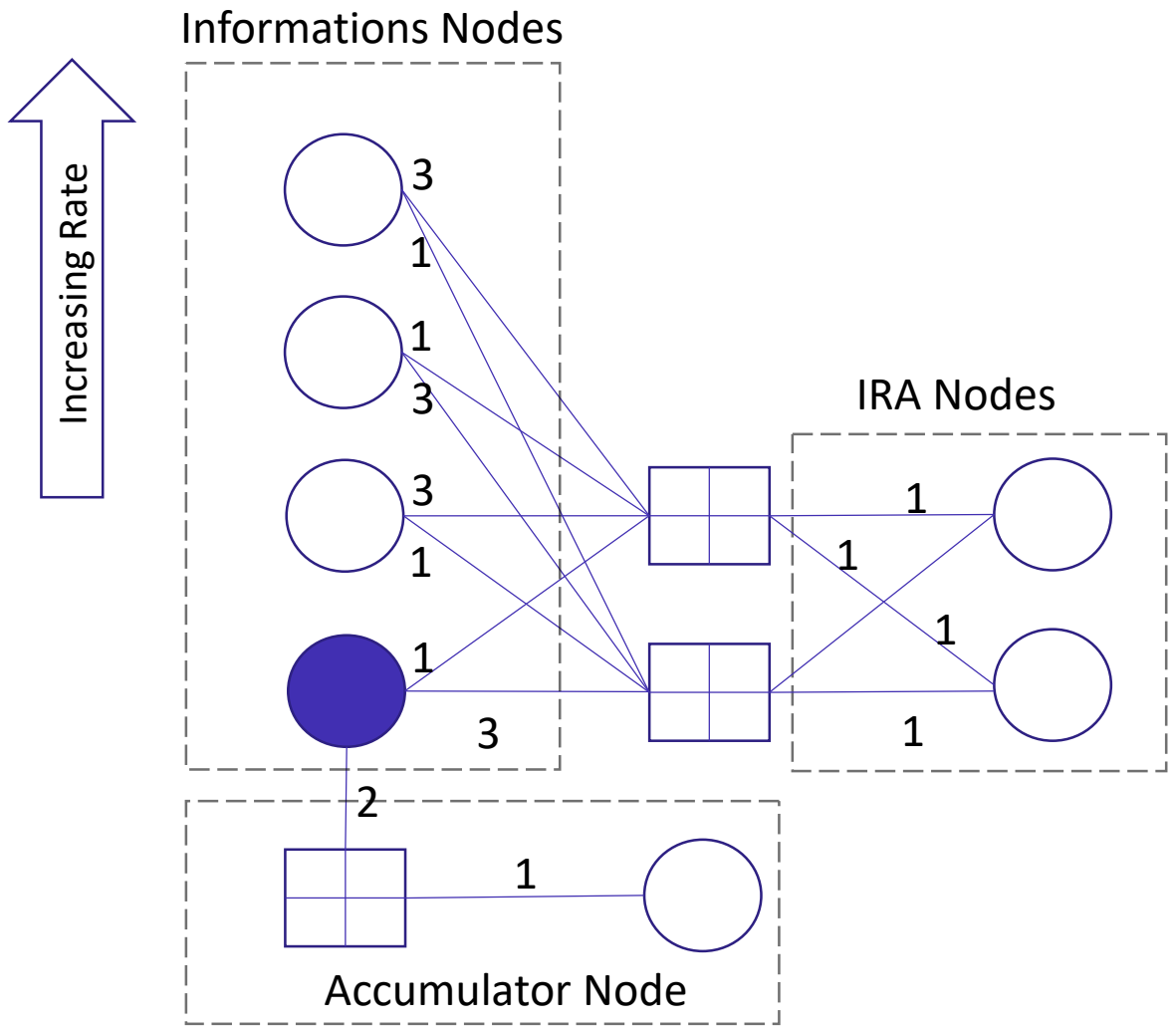
- ✓ Performant: decoding threshold close to Shannon limit
- ✓ Very low error (FER $\sim 1e^{-9}$ / $BER \sim 1e^{-12}$)
- ✓ Constant encoded size, to ease the framing and to maximize HW efficiency (one IP, multi-rate, same circulant size)
- ✓ Allowing to achieve 10Gbps encoded bits & 10GLLRs decoding with minimized complexity
- ✓ Flexibility with wide range of code rates (11 FEC codes : 9/10, 7/8 , 5/6, 4/5, 3/4, 2/3, 3/5, 1/2, 2/5, 3/8, 3/10)
- ✓ Code rates $R = 1/2$ and $R = 9/10$ are standardized in CCSDS LDPC O3K, CCSDS 142.0-B-1



2. ALGORITHM DESCRIPTION (1/2)

- In order to cope with HW constraints **IRA-Like** structure is suitable
- However, IRA codes performances decrease for low code rates and **show significant gap to theoretical limit** in that regime
- Lower code rate achieved thanks to Single Parity Check (SPC) extension (**Raptor-like design**)
- HW Encoder proven for **less than 5%** of a state of the art space qualified FPGA (detailed after)

Rate	Payload Size (k)	Punctured Size (N)
9/10	27648	30720
7/8	26880	30720
5/6	25600	30720
4/5	24576	30720
3/4	23040	30720
2/3	20480	30720
3/5	18432	30720
1/2	15360	30720
2/5	12288	30720
3/8	11520	30720
3/10	9216	30720



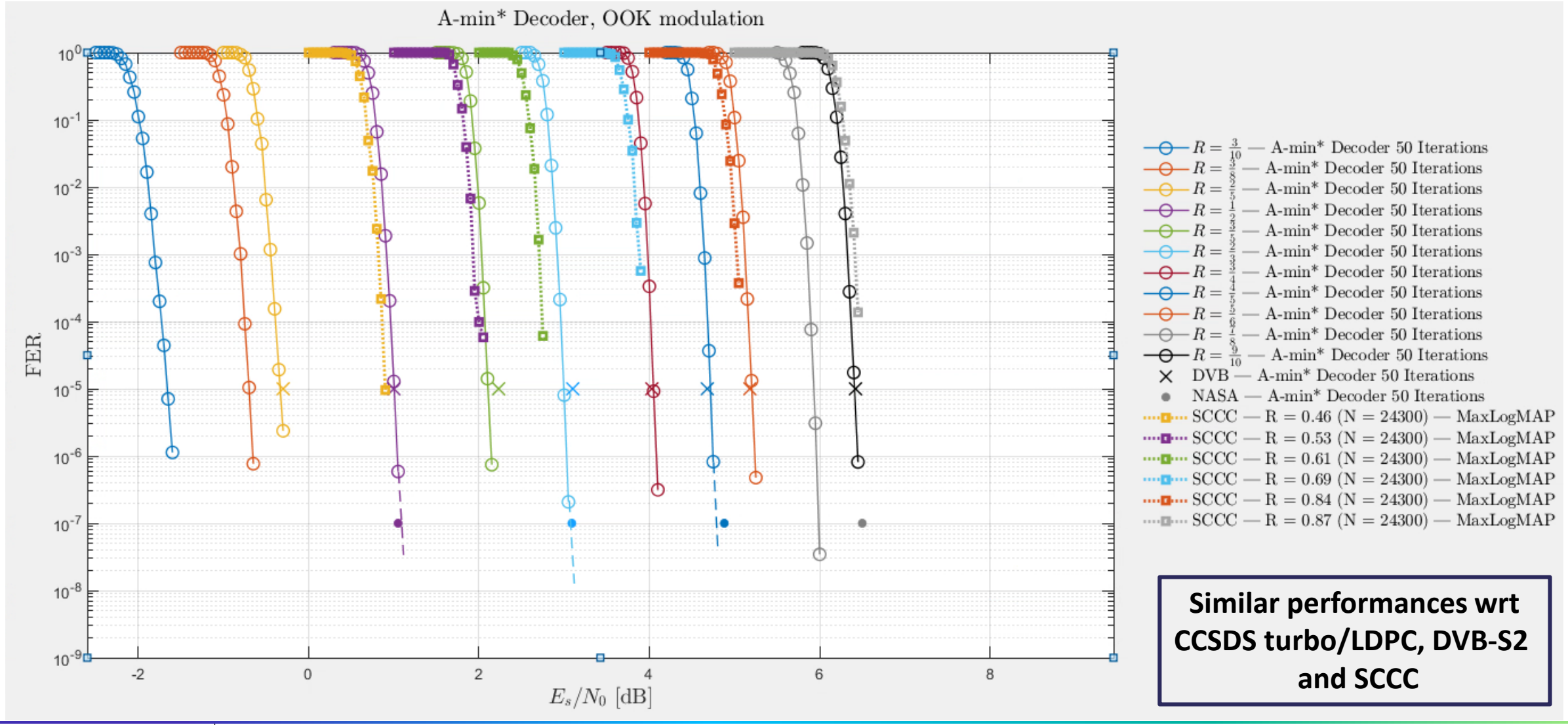
2. ALGORITHM DESCRIPTION (2/2)

LDPC Code Design

- SPC extension of photograph has been published in [1] & [2], achieving very good threshold
- Targeting very low error floor, this design is extended by the method of [3], to guarantee an upper bound on the photograph d_{min}
- The methodology has been published and validated in [4] with an FPGA implementation

[1] T. Chen, K. Vakilinia, D. Divsalar and R. D. Wesel, "Protograph-Based Raptor-Like LDPC Codes," in IEEE Transactions on Communications, vol. 63, no. 5, pp. 1522-1532, May 2015.
[2] T. V. Nguyen, A. Nosratinia and D. Divsalar, "The Design of Rate-Compatible Protograph LDPC Codes," in IEEE Transactions on Communications, vol. 60, no. 10, pp. 2841-2850, October 2012.
[3] S. V. S. Ranganathan, D. Divsalar and R. D. Wesel, "Design of improved quasi-cyclic protograph-based Raptor-like LDPC codes for short block-lengths," 2017 IEEE International Symposium on Information Theory (ISIT), Aachen, 2017, pp. 1207-1211.
[4] B. Gadat, L. Barthe, B. Matuz, C. Pouillat, "LDPC Codes with Low Errors and Efficient Encoders", in IEEE International Conference on Communications (ICC), May 2023.

3. PERFORMANCES (1/2)



Similar performances wrt CCSDS turbo/LDPC, DVB-S2 and SCCC

3. PERFORMANCES (2/2)

FPGA simulations of various codes using the standard OMS algorithm [4]

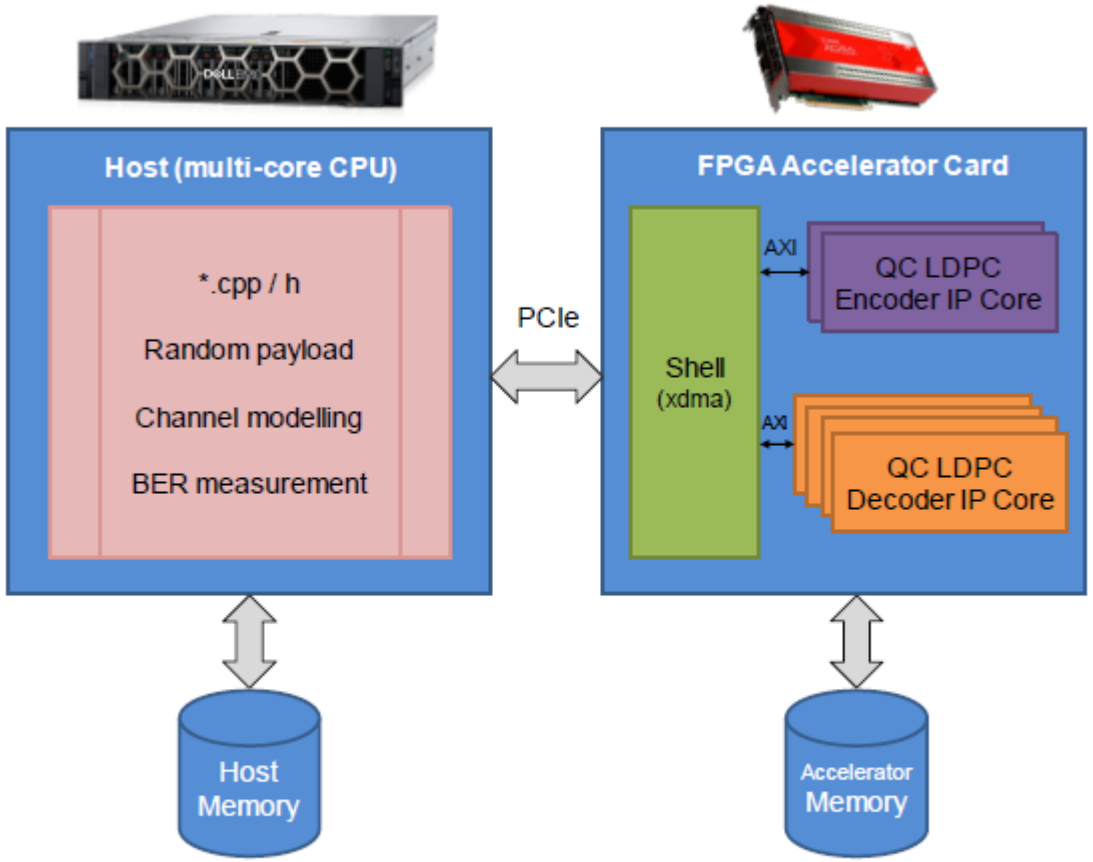
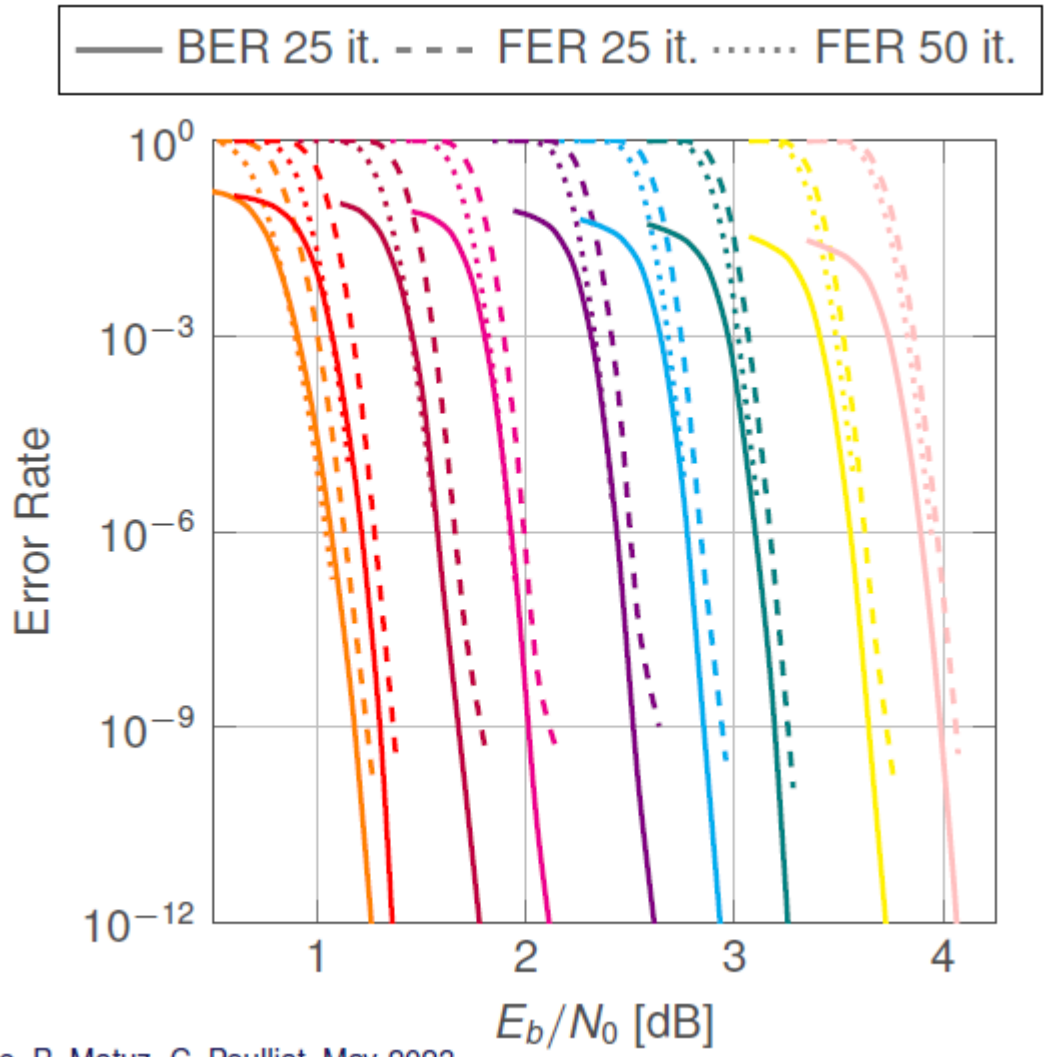


Figure: Simulation framework based on FPGA accelerator cards



LDPC Codes with Low Error Floors and Efficient Encoders, B. Gadat, L. Barthe, B. Matuz, C. Poulliat, May 2023

4. COMPLEXITY (1/3)

ENCODER COMPLEXITY - COMPARISON WITH COMPETITORS [4]

Normalized performances of encoders using a XCZU9EG FPGA

IP	LUT/Gbits	FF/Gbits	BRAM/Gbits
ADS O3K Enc.	298	393	1.647
DVB-S2 Enc.	4 063	3 146	3.059
ARJA Enc.	3 099	4046	0*

*: Full parallel architecture optimized for multi-gigabit applications. This approach saves internal memory blocks **but support only one code rate.**

4. COMPLEXITY (2/3)

DECODER COMPLEXITY - QUALITATIVE ANALYSIS

Although O3K codes were originally designed to reduce the on-board complexity of a satellite, i.e. the encoder part, they also benefit of modern LDPC code constructions for efficient HW implementation such as:

- **Full quasi cyclic (QC) structure**
  - → All interconnections between each photograph copy are described by full circular permutation matrices (not the case of DVB-S2X)
- **No code pathology**
  - → All circulant matrices are complete and single diagonal sub-matrices (not the case of DVB-S2X codes)
- **No interleaving/deinterleaving**:
  - → High throughput decoders for SATCOM applications don't take benefit of BICM for burst error decoding. By construction, the LDPC structure provides a robust interleaving scheme for AWGN or degraded AGWN channels, assuming typical NMS or OMS decoding algorithms
- **No outer code needed**:
  - → In the DVB-S2X standard, the BCH coding has been introduced to compensate high error floors of DVB-S2 LDPC codes. It adds complexity to the complete decoder but also introduces a constraint on possible code rates. DVB-S2X codes are therefore byte aligned, while O3K codes are at least 128-bit word aligned, which drastically reduces the complexity of hardware implementation for high data rates.
- **Fixed N strategy**:
  - → Unlike 5G codes, O3K codes are efficiently designed to address fixed bandwidth technologies such as SCPC links (feeders, PDT). This approach maximizes the usage of used HW resources for all code rates. For 5G codes, low rates dramatically increase the memory requirements.

4. COMPLEXITY (3/3)

DECODER COMPLEXITY – QUANTITATIVE ANALYSIS

About decoder implementation complexity, many parameters can influence the quantitative analysis.

The proposed implementation efficiently targets Xilinx' space grade FPGAs (Versal devices) using a multi-core design. It is based on standard horizontal layered OMS decoder cores with AXIS interfaces and early stopping criterion. The internal quantization is adapted to target at least a FER of 10^{-6} (like most DVB-S2X codes). The performances are normalized using a reference architecture that includes 11 code rates, from 3/10 to 9/10 (average results).

Normalized performances of decoders for 8 fixed iterations using a XQRVC1902(-1M) FPGA

IP	kLUT/GLLRs	kFF/GLLRs	BRAM/GLLRs	URAM/GLLRs
ADS O3K Dec.	~ 17	~ 18	~ 15	~ 9

5. CONCLUSION

The CCSDS LDPC O3K family code mainly offers

- Performance close to Shannon limit
- Low complexity for both encoder & decoder parts with very low error floor
- Wide range of code rates allowing high flexibility for ACM / VCM operations

CNES and ADS are making this presentation to share technical informations, and would welcome technical feed backs from other agencies on O3K LDPC codes in a potential RF context